DECLARATION

I, the undersigned, of 2-10, Mizuo 1-chome, Ibaraki-shi, Osaka, Japan, hereby certify that I am well acquainted with the English and Japanese languages, that I am an experienced translator for patent matter, and that the attached document is a true English translation of

Japanese Patent Application No. **9-21127**

that was filed in Japanese.

I declare that all statements made herein of my own knowledge are true, that all statements on information and belief are believed to be true, and that these statements were made with the knowledge that willful statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Signature:

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Dated: **August 4, 2004**

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[Name of the Document] SPECIFICATION

[Title of the Invention] SEMICONDUCTOR DEVICE AND PROCESS FOR FABRICATION OF THE SAME

[Claims]

[Claim 1] A semiconductor device comprising:

a substrate having a semiconductor region,

a first insulating film formed on said semiconductor region and having a property of reflowing due to a heat treatment under predetermined conditions,

a second insulating film formed on said first insulating film and containing at least silicon nitride, and

a shape-holding film formed at least either on top of or beneath said second insulating film and having a property of not reflowing due to the heat treatment under the predetermined conditions.

[Claim 2] A semiconductor device as set forth in Claim 1, wherein

said semiconductor device comprises: a first interconnect layer formed on said semiconductor region; a lower interlayer insulating film formed on said first interconnect layer and said semiconductor region; a second interconnect layer formed on said lower interlayer insulating film; and an upper interlayer insulating film formed on said second interconnect layer and said lower interlayer insulating film and having a property of reflowing due to the heat treatment under the predetermined conditions,

said first insulating film defines said lower interlayer insulating film,

said second insulating film covers the lower interlayer insulating film, and

said shape-holding film comprises an insulating film interposed between said interlayer insulating film and said capacitor insulating film.

[Claim 3] A semiconductor device as set forth in Claim 1 or 2, wherein

said second insulating film comprises a silicon nitride film.

[Claim 4] A semiconductor device as set forth in Claim 1, wherein

said semiconductor device is a stacked DRAM cell comprising a gate formed on said semiconductor region, an impurity diffusion layer formed in a region sideways of said gate in said semiconductor region, an interlayer insulating film formed on said gate and said semiconductor region, a storage node formed on said interlayer insulating film, a contact filling an opening formed in said interlayer insulating film and connecting said storage node to said impurity diffusion layer, a capacitor insulating film formed for coverage over said storage node and a part of said interlayer insulating film, and a plate electrode formed on said capacitor insulating film,

said first insulating film defines said interlayer insulating film,

said second insulating film defines said capacitor insulating film, and

said shape-holding film comprises an insulating film interposed between said interlayer insulating film and said capacitor insulating film.

[Claim 5] A semiconductor device as set forth in Claim 4, wherein

said second insulating film comprises a silicon nitride film.

[Claim 6] A semiconductor device as set forth in Claim 5, wherein

said plate electrode covers the whole surface of said capacitor insulating film.

[Claim 7] A semiconductor device as set forth in Claim 1, wherein

said semiconductor device is a stacked DRAM cell comprising a gate formed on said semiconductor region, an impurity diffusion layer formed in a region sideways of said gate in said semiconductor region, an interlayer insulating film formed on said gate and said semiconductor region, a storage node formed on said interlayer insulating film, a contact filling an opening formed in said interlayer insulating film and connecting said storage node to said impurity diffusion layer, a capacitor insulating film formed for coverage over said storage node and a part of said interlayer insulating film, and a plate electrode formed on said capacitor insulating film,

said first insulating film defines said interlayer insulating film,

said second insulating film defines said capacitor insulating film and comprises an

oxidized silicon nitride film formed by oxidizing a silicon nitride film,

said shape-holding film defines said plate electrode and covers the whole surface of said capacitor insulating film, and

said interlayer insulating film has a property of not reflowing due to a heat treatment for oxidizing said silicon nitride film.

[Claim 8] A semiconductor device as set forth in Claim 4, 5, 6, or 7, wherein

said storage node is a cylindrical storage node,

an silicon nitride film for an etching stopper is further provided immediately below said capacitor node, and

said capacitor insulating film is formed for coverage over surfaces of said storage node and said silicon nitride film for said etching stopper.

[Claim 9] A semiconductor device as set forth in Claim 8, wherein

a lower surface of said cylindrical storage node is spaced from the top surface of said silicon nitride film for said etching stopper, and

said capacitor insulating film is formed for coverage over surfaces of said cylindrical storage node, said contact and said etching stopper film.

[Claim 10] A semiconductor device as set forth in Claim 1, 2, 3, 4, 5, 6, 7, 8, or 9, wherein said first insulating film comprises a BPSG film.

[Claim 11] A semiconductor device as set forth in Claim 1, 2, 3, 4, or 5, wherein said shape-holding film comprises a silicon oxide film.

[Claim 12] A process for fabrication of a semiconductor device comprising the steps of:

depositing a lower interlayer insulating film on a semiconductor substrate, the lower interlayer insulating film having a property of reflowing due to a heat treatment under predetermined conditions;

causing said lower interlayer insulating film to reflow for planarization thereof by the heat treatment;

depositing a shape-holding insulating film on said lower interlayer insulating layer, said shape-holding insulating film having a property of not reflowing due to the heat treatment under the predetermined conditions;

laying an insulating film containing silicon nitride over said shape-holding insulating film;

depositing an upper interlayer insulating film on the insulating film containing silicon nitride, the upper interlayer insulating film having a property of reflowing due to a heat treatment under said predetermined conditions; and

causing said upper interlayer insulating film to reflow for planarization through the heat treatment under the predetermined conditions.

[Claim 13] A process for fabrication of a semiconductor device functioning as a stacked DRAM cell comprising the steps of:

depositing a lower interlayer insulating film on a semiconductor substrate, the lower interlayer insulating film having a property of reflowing due to a heat treatment under predetermined conditions;

causing said lower interlayer insulating film to reflow for planarization thereof by the heat treatment;

depositing a shape-holding insulating film on said lower interlayer insulating film, said shape-holding insulating film having a property of not reflowing due to a heat treatment under said predetermined conditions;

forming a contact hole extending through said shape-holding insulating film and said lower interlayer insulating film to said impurity diffusion layer;

depositing a polysilicon film on the whole surface of the substrate including said contact hole;

patterning said polysilicon film to form a storage node and a contact connecting said storage node to said impurity diffusion layer;

depositing a silicon nitride film on the whole surface of the substrate including the

exposed surface of the storage node; and

thermally oxidizing the silicon nitride film to form an oxidized silicon nitride film serving as a capacitor insulating film.

[Claim 14] A process for fabrication of a semiconductor device functioning as a stacked DRAM cell comprising the steps of:

depositing a lower interlayer insulating film on a semiconductor substrate, the lower interlayer insulating film having a property of reflowing due to a heat treatment under predetermined conditions;

causing said lower interlayer insulating film to reflow for planarization thereof by the heat treatment;

depositing a shape-holding insulating film on said lower interlayer insulating film, said shape-holding insulating film having a property of not reflowing due to a heat treatment under said predetermined conditions;

laying over said shape-holding insulating film an silicon nitride film for an etching stopper;

forming a contact hole extending through said silicon nitride film for said etching stopper, shape-holding insulating film and lower interlayer insulating film to said impurity diffusion layer;

depositing a first polysilicon film on the whole surface of the substrate including the contact hole;

patterning said silicon oxide films to form a core of a cylindrical storage node;

depositing a second polysilicon film on the whole surface of the substrate including an exposed surface of said core of said cylindrical storage node;

performing anisotropic etching on said first and second polysilicon films to remove parts of said first and second polysilicon films other than those on the sides of and beneath said core of said cylindrical storage node and form a cylindrical storage node and a contact connecting said cylindrical storage node and said impurity diffusion layer;

removing said core of the cylindrical storage node by etching;

thereafter depositing a silicon nitride film for a capacitor insulating film on the whole surface of the substrate; and

thermally oxidizing the silicon nitride film to form an oxidized silicon nitride film serving as a capacitor insulating film.

[Claim 15] A process for fabrication of a semiconductor device of Claim 13 or 14 further comprising the steps of:

patterning said oxidized silicon nitride film to form a capacitor insulating film;

depositing a conductor film on the whole surface of the substrate including an exposed surface of said capacitor insulating film and thereafter patterning said conductor film to form a plate electrode;

depositing an upper interlayer insulating film on the whole surface of the substrate after the formation of said plate electrode; and

performing heat treatment on said upper interlayer insulating film under predetermined conditions to cause said upper interlayer insulating film to reflow for planarization thereof.

[Claim 16] A process for fabrication of a semiconductor as set forth in Claim 14, wherein in said step of forming a core of said cylindrical storage node, a part of said first polysilicon film other than that located below said cylindrical storage node is also removed.

[Claim 17] A process for fabrication of a semiconductor as set forth in Claim 14, further including the step of forming a film for gap production on said silicon nitride film,

wherein in said step of forming a contact hole, said contact hole is formed to extend through said film for gap production as well,

in said step of forming a cylindrical storage node, said film for gap production is also removed to produce a gap between a lower surface of said cylindrical storage node and the top surface of said silicon nitride film for said etching stopper,

in said step of depositing a silicon nitride film, said silicon nitride film is deposited along the lower surface of said cylindrical storage node, side surfaces of said contact and the top surface of said silicon nitride film for said etching stopper.

[Claim 18] A process for fabrication of a semiconductor device functioning as a stacked DRAM cell comprising the steps of:

depositing a lower interlayer insulating film on a semiconductor substrate, the lower interlayer insulating film having a property of reflowing due to a heat treatment under predetermined conditions;

causing said lower interlayer insulating film to reflow for planarization thereof by the heat treatment;

forming a contact hole extending through lower interlayer insulating film to said impurity diffusion layer;

depositing a polysilicon film on the whole surface of the substrate including said contact hole;

patterning said polysilicon film to form a storage node and a contact connecting said storage node to said impurity diffusion layer;

depositing a silicon nitride film for a capacitor insulating film on the whole surface of the substrate including the exposed surface of the storage node;

thermally oxidizing the silicon nitride film for said capacitor insulating film to form an oxidized silicon nitride film;

depositing a conductor film on said oxidized silicon nitride film and thereafter patterning the conductor film to form a plate electrode;

removing a part of said oxidized silicon nitride film other than that below said plate electrode to form a capacitor insulating film;

thereafter depositing an upper interlayer insulating film on the whole surface of the substrate; and

performing heat treatment on said upper interlayer insulating film under

predetermined conditions to cause said upper interlayer insulating film to reflow for planarization thereof.

[Claim 19] A process for fabrication of a semiconductor device as set forth in Claim 18, further including the step of depositing a shape-holding insulating film on said lower interlayer insulating film after the step of planarizing said lower interlayer insulating film, said shape-holding insulating film having a property of not reflowing due to heat treatment under predetermined conditions,

wherein in the step of forming a contact hole, said contact hole is so formed as to extend through said shape-holding insulating film as well.

[Claim 20] A process for fabrication of a semiconductor device as set forth in Claim 18 or 19, further including, after the step of causing said lower interlayer insulating layer to reflow by heat treatment and thus planarizing said lower interlayer insulating layer, the step of depositing an insulating film for edge retention having a high etching selectivity to said lower interlayer insulating film,

wherein in said step of forming a contact hole, said contact hole is so formed as to extend through said insulating film for edge retention as well.

[Claim 21] A process for fabrication of a semiconductor device functioning as a cylindrical stacked DRAM cell comprising the steps of:

depositing a lower interlayer insulating film on a semiconductor substrate, the lower interlayer insulating film having a property of reflowing due to a heat treatment under predetermined conditions;

causing said lower interlayer insulating film to reflow for planarization thereof by the heat treatment;

forming a silicon nitride film for an etching stopper on said shape-holding insulating film;

forming a contact hole extending through said silicon nitride film for said etching stopper and lower interlayer insulating film to said impurity diffusion layer;

depositing a first polysilicon film on the whole surface of the substrate including said contact hole;

forming a silicon oxide film on said first polysilicon film;

patterning said silicon oxide film to form a core of a cylindrical storage node;

depositing a second polysilicon film on the whole surface of the substrate including an exposed surface of said core of said cylindrical storage node;

performing anisotropic etching on said first and second polysilicon films to remove parts of said first and second polysilicon films other than those on the sides of and beneath said core of said cylindrical storage node and form a cylindrical storage node and a contact connecting said cylindrical storage node and said impurity diffusion layer;

removing said core of the cylindrical storage node by etching;

thereafter depositing a silicon nitride film for a capacitor insulating film on the whole surface of the substrate;

thermally oxidizing the silicon nitride film for said capacitor insulating film to form an oxidized silicon nitride film;

depositing a conductor film on said oxidized silicon nitride film and thereafter patterning the conductor film to form a plate electrode;

removing parts of said oxidized silicon nitride film and silicon nitride film for the etching stopper other than those below said plate electrode to form a capacitor insulating film;

thereafter depositing an upper interlayer insulating film on the whole surface of the substrate; and

performing heat treatment on said upper interlayer insulating film under predetermined conditions to cause said upper interlayer insulating film to reflow for planarization thereof.

[Claim 22] A process for fabrication of a semiconductor device as set forth in Claim 21, wherein in said step of forming a core of said cylindrical storage node, said first

polysilicon film other than part thereof below said cylindrical storage node is also removed.

[Claim 23] A process for fabrication of a semiconductor as set forth in Claim 21, further including the step of forming a film for gap production on said silicon nitride film for said etching stopper,

wherein in said step of forming a contact hole, said contact hole is formed to extend through said film for gap production as well,

in said step of forming a cylindrical storage node, said film for gap production is also removed to produce a gap between a lower surface of said cylindrical storage node and the top surface of said silicon nitride film for said etching stopper,

in said step of depositing a silicon nitride film, said silicon nitride film is deposited along the lower surface of said cylindrical storage node, side surfaces of said contact and the top surface of said etching stopper silicon nitride film.

[Claim 24] A process for fabrication of a semiconductor device as set forth in Claim 21, 22 or 23, further including the step of depositing a shape-holding insulating film on said lower interlayer insulating film after the step of planarizing said lower interlayer insulating film, said shape-holding insulating film having a property of not reflowing due to heat treatment under predetermined conditions,

wherein in the step of forming a contact hole, said contact hole is so formed as to extend through said shape-holding insulating film as well.

[Claim 25] A process for fabrication of a semiconductor device as set forth in Claim 21, 22, 23, or 24, further including, after the step of causing said lower interlayer insulating layer to reflow by heat treatment and thus planarizing said lower interlayer insulating layer, the step of depositing an insulating film for edge retention having a high etching selectivity to said lower interlayer insulating film,

wherein in said step of forming a contact hole, said contact hole is so formed as to extend through said insulating film for edge retention as well.

[Claim 26] A process for fabrication of a semiconductor device functioning as a stacked DRAM cell comprising the steps of:

depositing a lower interlayer insulating film on a semiconductor substrate, the lower interlayer insulating film having a property of reflowing due to a heat treatment under predetermined conditions;

causing said lower interlayer insulating film to reflow for planarization thereof by the heat treatment;

forming a contact hole extending through said lower interlayer insulating film to said impurity diffusion layer;

depositing a polysilicon film on the whole surface of the substrate including said contact hole;

patterning said polysilicon film to form a storage node and a contact connecting said storage node and said impurity diffusion layer;

depositing a silicon nitride film for a capacitor insulating film on the whole surface of the substrate including an exposed surface of said storage node; and

thermally oxidizing the silicon nitride film for said capacitor insulating film to form an oxidized silicon nitride film,

wherein heat treatment conditions in the step of thermally oxidizing said silicon nitride film for the capacitor insulating film fall within the limitation of not allowing said lower interlayer insulating film to reflow.

[Claim 27] A process for fabrication of a semiconductor device as set forth in Claim 26, wherein

the heat treatment temperature for causing said lower interlayer insulating film to reflow is 830°C or more, and

the temperature at which said silicon nitride film for the capacitor insulating film is thermally oxidized is 820°C or less.

[Claim 28] A process for fabrication of a semiconductor device as set forth in

Claim 26, wherein said silicon nitride film for the capacitor insulating film is thermally oxidized in a dry atmosphere.

[Claim 29] A process for fabrication of a semiconductor device functioning as a stacked DRAM cell comprising the steps of:

depositing a lower interlayer insulating film on a semiconductor substrate, the lower interlayer insulating film having a property of reflowing due to a heat treatment under predetermined conditions;

causing said lower interlayer insulating film to reflow for planarization thereof by the heat treatment;

forming a contact hole extending through said lower interlayer insulating film to said impurity diffusion layer;

depositing a polysilicon film on the whole surface of the substrate including said contact hole;

patterning said polysilicon film to form a storage node and a contact connecting said storage node to said impurity diffusion layer;

nitriding an exposed surface of said lower interlayer insulating film;

depositing a silicon nitride film for a capacitor insulating film on the whole surface of the substrate including an exposed surface of said storage node, subsequently to the step of nitriding said lower interlayer insulating film; and

thermally oxidizing the silicon nitride film for said capacitor insulating film to form an oxidized silicon nitride film.

[Claim 30] A process for fabrication of a semiconductor device as set forth in Claim 29, wherein in the step of nitriding the surface of said lower interlayer insulating film, heat treatment is performed in an atmosphere of nitrogen or ammonia.

[Claim 31] A process for fabrication of a semiconductor device functioning as a stacked DRAM cell comprising the steps of:

depositing a lower interlayer insulating film made of a BPSG film on a

semiconductor substrate, the lower interlayer insulating film having a property of not reflowing due to a heat treatment under predetermined conditions;

causing said lower interlayer insulating film to reflow for planarization thereof by the heat treatment;

forming a contact hole extending through said lower interlayer insulating film to said impurity diffusion layer;

depositing a polysilicon film on the whole surface of the substrate including said contact hole;

patterning said polysilicon film to form a storage node and a contact connecting said storage node to said impurity diffusion layer;

depositing a silicon nitride film for a capacitor insulating film on the whole surface of the substrate including an exposed surface of said storage node; and

thermally oxidizing the silicon nitride film for said capacitor insulating film to form an oxidized silicon nitride film.

[Claim 32] A process for fabrication of a semiconductor device as set forth in Claim 31, wherein the BPSG film contains, as impurities, 5.0 wt% or less of phosphorus and 6.0 wt% or less of boron.

[Claim 33] A process for fabrication of a semiconductor device as set forth in Claim 26, 19, or 31, wherein a cylindrical storage node is formed as said storage node.

[Detailed Description of the Invention]

[Technical Field to which the Invention Belongs]

The present invention generally relates to a semiconductor device comprising a substrate and an interlayer insulating film having a thermally reflowable property and a fabrication process therefor, and more particularly to a countermeasure against deformation of a nitride film overlying the interlayer insulating film.

[Prior Art]

With progress toward high-integration, the prior-art semiconductor device has an

increasing number of interconnection layers formed on the substrate. Accordingly, it is common practice in the art to perform a process comprising the steps of laying a first BPSG film over a first interconnection layer, followed by heat treating the first BPSG film for planarization thereof, and forming a second interconnection layer and then a second BPSG film on the first BPSG film, followed by planarization of the second BPSG film. This process has a drawback that when the second BPSG film is heat treated, the first BPSG film is also caused to reflow and dislocation of the second interconnection layer results. As prevention against this problem, a process including a step to lay a silicon nitride film over the first BPSG film is disclosed in Laid Open Unexamined Japanese Patent Publication No.5(1993)-160276.

Fig. 16 is a sectional view showing an example of the prior-art semiconductor device including such a silicon nitride film for prevention against the reflow of the second interconnection layer. As seen in Fig. 16, the semiconductor device is arranged such that a transistor gate 47 as the first interconnection layer is formed on a silicon substrate, a first BPSG film 48 as the first interlayer insulating film laid over the gate 47, a polycide interconnection 49 as the second interconnection layer formed on the first BPSG film 48. Formed on the first BPSG film 48 is a polycide interconnection 49 as the second interconnection layer. A protective silicon nitride film 50 is laid over the first BPSG film 48 for the purpose of preventing the reflow and oxidation of the first BPSG film and subsequently, a second BPSG film 51 as the second interlayer insulating film is laid over the silicon nitride film 50. This process is designed to utilize the silicon nitride film 50 for blocking vapor during the heat treatment for planarizing the second BPSG film 51 in an atmosphere of vapor, thereby preventing the reflow of the first BPSG film 48 and thus avoiding defects caused by dislocation of the polycide interconnection 49.

A method of fabricating a stacked DRAM cell often utilizes an oxidized silicon nitride film as a capacitor insulating film generally presenting prescribed properties such as refresh, isolation voltage and the like. Further, the BPSG film is often utilized for

planarizing the base of a storage node.

Now referring to Fig. 17, a brief description will be made on the prior-art stacked DRAM structure. As seen in Fig. 17, the stacked DRAM structure comprises a silicon substrate 1, an overlying BPSG film 52 reflowable by a heat treatment at low temperatures, a storage node 54, a contact 53 for connecting the storage node 54 to an impurity diffusion layer in the silicon substrate 1, an oxidized silicon nitride film 55 serving as the capacitor insulating film, and a plate electrode 56. In such a structure, the oxidized silicon nitride film 55 as the capacitor insulating film exists partially on the BPSG film 52.

In addition, there is proposed a stacked DRAM structure including a cylindrical storage node for increasing the surface area of the storage node.

As seen in Fig. 18, this structure comprises a silicon substrate 1, a BPSG film 57 reflowable by a heat treatment at low temperatures, a silicon nitride film 58 serving as a wet etching stopper, a cylindrical storage node 60, a contact 59 for connecting the cylindrical storage node 60 to an impurity diffusion layer in the substrate 1, an oxidized silicon nitride film 61 serving as the capacitor insulating film, and a plate electrode 62. In this structure, as well, the oxidized silicon nitride film 61 as the capacitor insulating film exists partially on the BPSG film 57.

[Problems that the Invention is to solve]

The aforementioned semiconductor devices known to the art have the following problems.

More recently, in response to a demand for fabricating a semiconductor device at lower temperatures, the BPSG film need be heat treated at lower temperatures. In order that such a low-temperature heat treatment may accomplish a similar flow and forming of the film to that offered by the heat treatment practiced in the art, the BPSG film contains boron and phosphorus in high concentrations. With the use of such a high-concentration BPSG film, the process wherein the silicon nitride film is deposited and oxidized to obtain the oxidized silicon nitride film shown in Fig. 17 or 18 have a drawback that a first BPSG

film 63 tends to reflow so readily as to produce wrinkle in the silicon nitride film 64, as shown in Fig. 19(A). The inventors of the present invention have found from experiments that the wrinkle tends to occur at a wide area with a low density of memory cells as well as at place under which a step in the first BPSG film 63 as the base is located. It was also found that as the thickness of the silicon nitride film 64 as the capacitor insulating film decreases, the incidence of wrinkle becomes greater.

Further investigation demonstrated that in case where the silicon nitride film is thick, particularly where the cylindrical storage node 60 is formed, as shown in Fig. 18, and the silicon nitride film 58 is used as the wet etching stopper, a silicon nitride film 66 may suffer the occurrence of cracks therein, as shown in Fig. 19.

It was also found that even in a structure including the silicon nitride film 50 shown in Fig. 16, the heat treatment for planarizing the second BPSG film 51 may disadvantageously produce a partial reflow of the first BPSG film 48, thus involving a danger of producing the aforesaid wrinkle or cracks in the silicon nitride film. Supposedly, this may be because the silicon nitride film 50 does not completely block vapor penetrating therethrough downward but rather allows an amount of gases, such as vapor, to penetrate therethrough.

Hence, the conventional technique cannot ensure that even a part of the silicon nitride film does not suffer the occurrence of wrinkle or cracks therein in case where after the planarization of the interlayer insulating layer, such as BPSG film having a thermally planarizable property, one of various steps requiring the semiconductor substrate to be kept heated, such as heat treatment for planarizing the upper interlayer insulating film and thermal oxidation, is performed.

The present invention is made to solve the above problems, and its object is to provide a semiconductor device and a fabrication process therefor which are adapted to prevent the occurrence of wrinkle or cracks in the silicon nitride film despite a degree of reflow of the BPSG film in case where an interlayer insulating film such as a BPSG film

heavily doped with impurities is employed and a subsequent step requires treatment under a high temperature condition.

[Means of Solving the Problems]

In order to achieve the above object, the present invention takes the countermeasures on semiconductor devices of Claims 1 through 11 and the countermeasures on processes for fabrication of the same of Claims 12 through 33.

As defined in Claim 1, a semiconductor device of the present invention comprises: a substrate having a semiconductor region, a first insulating film formed on said semiconductor region and having a property of reflowing due to a heat treatment under predetermined conditions, a second insulating film formed on said first insulating film and containing at least silicon nitride, and a shape-holding film formed at least either on top of or beneath said second insulating film and having a property of not reflowing due to the heat treatment under the predetermined conditions.

With this structure, even if in the process for fabricating the semiconductor device, a heat treatment under the predetermined conditions is performed after the formation of the second insulating film thereby causing the first insulating film at a lower level to reflow, the second insulating film does not suffer the occurrence of wrinkle or cracks therein because the second insulating film is supported by the shape-holding film having a property of not reflowing under predetermined conditions. This leads to the prevention of defective products due to wrinkle or cracks occurred in the second insulating film and hence, an enhanced yield and reliability of the semiconductor devices results. Additionally, the invention allows the planarization of the first insulating film to be performed at lower temperatures, thus contributing to improved performance of the semiconductor device.

As defined in Claim 2, in the device of Claim 1, said semiconductor device may comprise: a first interconnect layer formed on said semiconductor region; a lower interlayer insulating film formed on said first interconnect layer and said semiconductor

region; a second interconnect layer formed on said lower interlayer insulating film; and an upper interlayer insulating film formed on said second interconnect layer and said lower interlayer insulating film and having a property of reflowing due to the heat treatment under the predetermined conditions, said first insulating film may define said lower interlayer insulating film, said second insulating film may cover the lower interlayer insulating film, and said shape-holding film may comprise an insulating film interposed between said interlayer insulating film and said capacitor insulating film.

With this structure, even if in the process for fabricating the semiconductor device, the upper interlayer insulating film is allowed to reflow and thereby is planarized, the second insulating film does not suffer the occurrence of wrinkle or cracks therein. This provides a semiconductor device having good flatness as a whole and high performance and reliability.

As defined in Claim 3, in the device of Claim 1 or 2, the second insulating film may comprise a silicon nitride film.

This structure assures prevention of the occurrence of wrinkle or cracks in the second insulating film if the fabrication process for semiconductor device includes a step to oxidize the a silicon nitride film composing the second insulating film for obtaining the oxidized silicon nitride film and therefore, a semiconductor device featuring good flatness as a whole as well as high performance and reliability is provided.

As defined in Claim 4, in the device of Claim 1, said semiconductor device may be a stacked DRAM cell comprising a gate formed on said semiconductor region, an impurity diffusion layer formed in a region sideways of said gate in said semiconductor region, an interlayer insulating film formed on said gate and said semiconductor region, a storage node formed on said interlayer insulating film, a contact filling an opening formed in said interlayer insulating film and connecting said storage node to said impurity diffusion layer, a capacitor insulating film formed for coverage over said storage node and a part of said interlayer insulating film, and a plate electrode formed on said capacitor insulating film,

said first insulating film may define said interlayer insulating film, said second insulating film may define said capacitor insulating film, and said shape-holding film may comprise an insulating film interposed between said interlayer insulating film and said capacitor insulating film.

With this structure, the effect of Claim 1 provides a stacked DRAM cell free from wrinkle or cracks in the capacitor insulating film and featuring high performance and reliability.

As defined in Claim 5, in the device of Claim 4, said second insulating film may comprise a silicon nitride film.

With this structure, a semiconductor device is obtained which is free from wrinkle or cracks in the capacitor insulating film due to the heat treatment for the formation of the capacitor insulating film and features high performance and reliability, while a capacitor insulating film is provided which features good bondability with the plate electrode and properly adjusted dielectric properties.

As defined in Claim 6, in the device of Claim 5, said plate electrode may cover the whole surface of said capacitor insulating film.

With this structure, the capacitor insulating film does not suffer the occurrence of wrinkle or cracks therein because the capacitor insulating film is also supported by the plate electrode.

As defined in Claim 7, in the device of Claim 1, said semiconductor device may be a stacked DRAM cell comprising a gate formed on said semiconductor region, an impurity diffusion layer formed in a region sideways of said gate in said semiconductor region, an interlayer insulating film formed on said gate and said semiconductor region, a storage node formed on said interlayer insulating film, a contact filling an opening formed in said interlayer insulating film and connecting said storage node to said impurity diffusion layer, a capacitor insulating film formed for coverage over said storage node and a part of said interlayer insulating film, and a plate electrode formed on said capacitor insulating film,

said first insulating film may define said interlayer insulating film, said second insulating film may define said capacitor insulating film and comprise an oxidized silicon nitride film formed by oxidizing a silicon nitride film, said shape-holding film may define said plate electrode and cover the whole surface of said capacitor insulating film, and said interlayer insulating film may have a property of not reflowing due to a heat treatment for oxidizing said silicon nitride film.

This structure assures the prevention of occurrence of wrinkle or the like in the silicon nitride film if the fabrication process for the stacked DRAM cell includes the step of thermally oxidizing the silicon nitride film for obtaining the oxidized silicon nitride film. Even if an interlayer insulating film having a thermally reflowable property is further provided at a higher level, the capacitor insulating film does not suffer the occurrence of wrinkle or cracks therein because the capacitor insulating film is supported by the overlying plate electrode during the planarization of the upper interlayer insulating film. Thus is provided a stacked DRAM cell free from wrinkle or cracks in the capacitor insulating film and featuring high performance and reliability.

As defined in Claim 8, in the device of Claim 4, 5, 6, or 7, said storage node may be a cylindrical storage node, an silicon nitride film for an etching stopper may be further provided immediately below said capacitor node, and said capacitor insulating film may be formed for coverage over surfaces of said storage node and said silicon nitride film for said etching stopper.

With this structure, a stacked DRAM cell is provided which is free from wrinkle or cracks in the capacitor insulating film and features high performance and reliability.

As defined in Claim 9, in the device of Claim 8, a lower surface of said cylindrical storage node may be spaced from the top surface of said silicon nitride film for said etching stopper, and said capacitor insulating film may be formed for coverage over surfaces of said cylindrical storage node, said contact and said etching stopper film.

This structure increases the total area of the capacitor insulating film, thus offering

a cylindrical stacked DRAM cell featuring excellent refresh characteristic without isolation voltage decrease.

As defined in Claim 10, in the device of Claim 1, 2, 3, 4, 5, 6, 7, 8, or 9, said first insulating film preferably comprises a BPSG film.

This structure can make advantage of the BPSG film reflowable at low temperatures to offer a semiconductor device having the first insulating film with good flatness and featuring high performance and reliability.

As defined in Claim 11, in the device of Claim 1, 2, 3, 4, or 5, said shape-holding film preferably comprises a silicon oxide film.

This structure can make advantage of the silicon oxide film being readily formed and not adversely affecting the properties of the semiconductor device to offer a semiconductor device featuring high performance and reliability and low cost fabrication.

As defined in Claim 12, a first process for fabrication of a semiconductor device comprises the steps of: depositing a lower interlayer insulating film on a semiconductor substrate, the lower interlayer insulating film having a property of reflowing due to a heat treatment under predetermined conditions; causing said lower interlayer insulating film to reflow for planarization thereof by the heat treatment; depositing a shape-holding insulating film on said lower interlayer insulating layer, said shape-holding insulating film having a property of not reflowing due to the heat treatment under the predetermined conditions; laying an insulating film containing silicon nitride over said shape-holding insulating film; depositing an upper interlayer insulating film on the insulating film containing silicon nitride, the upper interlayer insulating film having a property of reflowing due to a heat treatment under said predetermined conditions; and causing said upper interlayer insulating film to reflow for planarization through the heat treatment under the predetermined conditions.

According to this process, at least a part of the lower interlayer insulating film is likely to reflow because heat treatment is performed, in the step of planarizing the upper

interlayer insulating film, under predetermined conditions. Even if the lower interlayer insulating film reflows, the insulating film containing silicon nitride is supported by the shape-holding insulating film. This prevents the occurrence of wrinkle or cracks in the insulating film containing silicon nitride. Thus, a semiconductor device featuring high performance and reliability can be formed.

As defined in Claim 13, a second process for fabrication of a semiconductor device functioning as a stacked DRAM cell comprises the steps of: depositing a lower interlayer insulating film on a semiconductor substrate, the lower interlayer insulating film having a property of reflowing due to a heat treatment under predetermined conditions; causing said lower interlayer insulating film to reflow for planarization thereof by the heat treatment; depositing a shape-holding insulating film on said lower interlayer insulating film, said shape-holding insulating film having a property of not reflowing due to a heat treatment under said predetermined conditions; forming a contact hole extending through said shape-holding insulating film and said lower interlayer insulating film to said impurity diffusion layer; depositing a polysilicon film on the whole surface of the substrate including said contact hole; patterning said polysilicon film to form a storage node and a contact connecting said storage node to said impurity diffusion layer; depositing a silicon nitride film on the whole surface of the substrate including the exposed surface of the storage node; and thermally oxidizing the silicon nitride film to form an oxidized silicon nitride film serving as a capacitor insulating film.

According to this process, despite a fear that the thermal oxidation of the silicon nitride film may cause the lower interlayer insulating film to reflow during the formation of the oxidized silicon nitride film constituting the capacitor insulating film for stacked DRAM cell, the shape-holding insulating film existing on the lower interlayer insulating film prevents the occurrence of wrinkle or cracks in the silicon nitride film located thereon. Thus, a semiconductor device featuring excellent memory characteristic and high reliability can be formed.

As defined in Claim 14, a third process for fabrication of a semiconductor device functioning as a stacked DRAM cell comprises the steps of: depositing a lower interlayer insulating film on a semiconductor substrate, the lower interlayer insulating film having a property of reflowing due to a heat treatment under predetermined conditions; causing said lower interlayer insulating film to reflow for planarization thereof by the heat treatment; depositing a shape-holding insulating film on said lower interlayer insulating film, said shape-holding insulating film having a property of not reflowing due to a heat treatment under said predetermined conditions; laying over said shape-holding insulating film an silicon nitride film for an etching stopper; forming a contact hole extending through said silicon nitride film for said etching stopper, shape-holding insulating film and lower interlayer insulating film and to said impurity diffusion layer; depositing a first polysilicon film on the whole surface of the substrate including the contact hole; patterning said silicon oxide films to form a core of a cylindrical storage node; depositing a second polysilicon film on the whole surface of the substrate including an exposed surface of said core of said cylindrical storage node; performing anisotropic etching on said first and second polysilicon films to remove parts of said first and second polysilicon films other than those on the sides of and beneath said core of said cylindrical storage node and form a cylindrical storage node and a contact connecting said cylindrical storage node and said impurity diffusion layer; removing said core of the cylindrical storage node by etching; thereafter depositing a silicon nitride film for a capacitor insulating film on the whole surface of the substrate; and thermally oxidizing the silicon nitride film to form an oxidized silicon nitride film serving as a capacitor insulating film.

According to this process, even if the lower interlayer insulating film reflows, wrinkle or cracks is not produced in the silicon nitride film for the capacitor insulating film and the silicon nitride film for the etching stopper. The reason for this is that the shape-holding insulating film is formed on the lower interlayer insulating film when the step of thermally oxidizing the silicon nitride film for the capacitor insulating film is

carried out. Thus, the cylindrical storage node can smoothly be formed, and a semiconductor device can be formed which features excellent memory characteristic and high reliability.

As defined in Claim 15, in the process of Claim 13 or 14, a process for fabrication of a semiconductor device may further comprise the steps of: patterning said oxidized silicon nitride film to form a capacitor insulating film; depositing a conductor film on the whole surface of the substrate including an exposed surface of said capacitor insulating film and thereafter patterning said conductor film to form a plate electrode; depositing an upper interlayer insulating film on the whole surface of the substrate after the formation of said plate electrode; and performing heat treatment on said upper interlayer insulating film under predetermined conditions to cause said upper interlayer insulating film to reflow for planarization thereof.

According to this process, even if the lower interlayer insulating film reflows in the step of forming the upper interlayer insulating film, the above-described effect of supporting the shape-holding insulating film prevents the occurrence of wrinkle or cracks in the silicon nitride film for the capacitor insulating film and the silicon nitride film for the etching stopper.

As defined in Claim 16, in the process of Claim 14, in said step of forming a core of said cylindrical storage node, a part of said first polysilicon film other than that located below said cylindrical storage node may also be removed.

As defined in Claim 17, in the process of Claim 14, a process for fabrication of a semiconductor may further include the step of forming a film for gap production on said silicon nitride film, wherein in said step of forming a contact hole, said contact hole may be formed to extend through said film for gap production as well, in said step of forming a cylindrical storage node, said film for gap production may also be removed to produce a gap between a lower surface of said cylindrical storage node and the top surface of said silicon nitride film for said etching stopper, in said step of depositing a silicon nitride film,

said silicon nitride film may be deposited along the lower surface of said cylindrical storage node, side surfaces of said contact and the top surface of said silicon nitride film for said etching stopper.

This process provides a cylindrical stacked DRAM cell featuring long retention time, good refresh characteristic and the like, without isolation voltage decrease.

As defined in Claim 18, a fourth process for fabrication of a semiconductor device functioning as a stacked DRAM cell comprises the steps of: depositing a lower interlayer insulating film on a semiconductor substrate, the lower interlayer insulating film having a property of reflowing due to a heat treatment under predetermined conditions; causing said lower interlayer insulating film to reflow for planarization thereof by the heat treatment; forming a contact hole extending through lower interlayer insulating film to said impurity diffusion layer; depositing a polysilicon film on the whole surface of the substrate including said contact hole; patterning said polysilicon film to form a storage node and a contact connecting said storage node to said impurity diffusion layer; depositing a silicon nitride film for a capacitor insulating film on the whole surface of the substrate including the exposed surface of the storage node; thermally oxidizing the silicon nitride film for said capacitor insulating film to form an oxidized silicon nitride film; depositing a conductor film on said oxidized silicon nitride film and thereafter patterning the conductor film to form a plate electrode; removing a part of said oxidized silicon nitride film other than that below said plate electrode to form a capacitor insulating film; thereafter depositing an upper interlayer insulating film on the whole surface of the substrate; and performing heat treatment on said upper interlayer insulating film under predetermined conditions to cause said upper interlayer insulating film to reflow for planarization thereof.

According to this process, in the step of planarizing the upper interlayer insulating film, even if the lower interlayer insulating film reflows, the coverage of the plate electrode over the whole surface of capacitor insulating film prevents wrinkle or cracks also in a part of the capacitor insulating film. Thus, a stacked DRAM cell can be formed which

features excellent memory characteristic and high reliability.

As defined in Claim 19, in the process of Claim 18, a process for fabrication of a semiconductor device may further include the step of depositing a shape-holding insulating film on said lower interlayer insulating film after the step of planarizing said lower interlayer insulating film, said shape-holding insulating film having a property of not reflowing due to heat treatment under predetermined conditions, wherein in the step of forming a contact hole, said contact hole may be so formed as to extend through said shape-holding insulating film as well.

With this process, also in the step of oxidizing the silicon nitride film for the capacitor insulating film, the occurrence of wrinkle or cracks due to the reflow of the lower interlayer insulating film can certainly be prevented in the silicon nitride film for the capacitor insulating film.

As defined in Claim 20, in the process of Claim 18 or 19, the process for fabrication of a semiconductor device may further include, after the step of causing said lower interlayer insulating layer to reflow by heat treatment and thus planarizing said lower interlayer insulating layer, the step of depositing an insulating film for edge retention having a high etching selectivity to said lower interlayer insulating film, wherein in said step of forming a contact hole, said contact hole may be so formed as to extend through said insulating film for edge retention as well.

This process assuredly prevents the step of forming the contact hole from forming a contact hole with a chipped edge, which results in an increased size of the contact hole.

As defined in Claim 21, a fifth process for fabrication of a semiconductor device functioning as a cylindrical stacked DRAM cell comprises the steps of: depositing a lower interlayer insulating film on a semiconductor substrate, the lower interlayer insulating film having a property of reflowing due to a heat treatment under predetermined conditions; causing said lower interlayer insulating film to reflow for planarization thereof by the heat treatment; forming a silicon nitride film for an etching stopper on said shape-holding

insulating film; forming a contact hole extending through said silicon nitride film for said etching stopper and lower interlayer insulating film to said impurity diffusion layer; depositing a first polysilicon film on the whole surface of the substrate including said contact hole; forming a silicon oxide film on said first polysilicon film; patterning said silicon oxide film to form a core of a cylindrical storage node; depositing a second polysilicon film on the whole surface of the substrate including an exposed surface of said core of said cylindrical storage node; performing anisotropic etching on said first and second polysilicon films to remove parts of said first and second polysilicon films other than those on the sides of and beneath said core of said cylindrical storage node and form a cylindrical storage node and a contact connecting said cylindrical storage node and said impurity diffusion layer; removing said core of the cylindrical storage node by etching; thereafter depositing a silicon nitride film for a capacitor insulating film on the whole surface of the substrate; thermally oxidizing the silicon nitride film for said capacitor insulating film to form an oxidized silicon nitride film; depositing a conductor film on said oxidized silicon nitride film and thereafter patterning the conductor film to form a plate electrode; removing parts of said oxidized silicon nitride film and silicon nitride film for the etching stopper other than those below said plate electrode to form a capacitor insulating film; thereafter depositing an upper interlayer insulating film on the whole surface of the substrate; and performing heat treatment on said upper interlayer insulating film under predetermined conditions to cause said upper interlayer insulating film to reflow for planarization thereof.

According to this process, in the step of planarizing the upper interlayer insulating film, even if the lower interlayer insulating film reflows, the coverage of the plate electrode over the whole surface of capacitor insulating film prevents the occurrence of wrinkle or cracks also in a part of the capacitor insulating film. Thus, a cylindrical stacked DRAM cell can be formed which features excellent memory characteristic and high reliability.

As defined in Claim 22, in the process of Claim 21, in said step of forming a core

of said cylindrical storage node, said first polysilicon film other than part thereof below said cylindrical storage node may also be removed.

As defined in Claim 23, in the process of Claim 21, the process for fabrication of a semiconductor may further include the step of forming a film for gap production on said silicon nitride film for said etching stopper, wherein in said step of forming a contact hole, said contact hole may be formed to extend through said film for gap production as well, in said step of forming a cylindrical storage node, said film for gap production may also be removed to produce a gap between a lower surface of said cylindrical storage node and the top surface of said silicon nitride film for said etching stopper, in said step of depositing a silicon nitride film, said silicon nitride film may be deposited along the lower surface of said cylindrical storage node, side surfaces of said contact and the top surface of said etching stopper silicon nitride film.

This process provides a cylindrical stacked DRAM cell featuring long retention time, good refresh characteristic and the like, without isolation voltage decrease.

As defined in Claim 24, in the process of Claim 21, 22, or 23, the process for fabrication of a semiconductor device may further include the step of depositing a shape-holding insulating film on said lower interlayer insulating film after the step of planarizing said lower interlayer insulating film, said shape-holding insulating film having a property of not reflowing due to heat treatment under predetermined conditions, wherein in the step of forming a contact hole, said contact hole may be so formed as to extend through said shape-holding insulating film as well.

According to this process, in the step of thermally oxidizing the silicon nitride film for the capacitor insulating film to form the oxidized silicon nitride film, even if the lower interlayer insulating film reflows, the occurrence of wrinkle or cracks due to this reflow can be certainly prevented in the oxidized silicon nitride film for the capacitor insulating film.

As defined in Claim 25, in the process of Claim 21, 22, 23, or 24, the process for

fabrication of a semiconductor device may further include, after the step of causing said lower interlayer insulating layer to reflow by heat treatment and thus planarizing said lower interlayer insulating layer, the step of depositing an insulating film for edge retention having a high etching selectivity to said lower interlayer insulating film, wherein in said step of forming a contact hole, said contact hole may be so formed as to extend through said insulating film for edge retention as well.

This process assuredly prevents the step of forming a contact hole from forming a contact hole with a chipped edge, which results in an increased size of the contact hole.

As defined in Claim 26, a sixth process for fabrication of a semiconductor device functioning as a stacked DRAM cell comprises the steps of: depositing a lower interlayer insulating film on a semiconductor substrate, the lower interlayer insulating film having a property of reflowing due to a heat treatment under predetermined conditions; causing said lower interlayer insulating film to reflow for planarization thereof by the heat treatment; forming a contact hole extending through said lower interlayer insulating film to said impurity diffusion layer; depositing a polysilicon film on the whole surface of the substrate including said contact hole; patterning said polysilicon film to form a storage node and a contact connecting said storage node and said impurity diffusion layer; depositing a silicon nitride film for a capacitor insulating film on the whole surface of the substrate including an exposed surface of said storage node; and thermally oxidizing the silicon nitride film for said capacitor insulating film to form an oxidized silicon nitride film, wherein heat treatment conditions in the step of thermally oxidizing said silicon nitride film for the capacitor insulating film fall within the limitation of not allowing said lower interlayer insulating film to reflow.

According to this process, in the step of thermally oxidizing the silicon nitride film for the capacitor insulating film, the first interlayer insulating film does not reflow. This can certainly prevent the occurrence of wrinkle or cracks of the silicon nitride film during thermal oxidation.

As defined in Claim 27, in the process of Claim 26, the heat treatment temperature for causing said lower interlayer insulating film to reflow may be 830°C or more, and the temperature at which said silicon nitride film for the capacitor insulating film is thermally oxidized may be 820°C or less.

As defined in Claim 30, in the process of Claim 28, said silicon nitride film for the capacitor insulating film may thermally be oxidized in a dry atmosphere.

This method can make advantage of the fact that the first insulating film is harder to reflow in dry atmosphere than in a pyrogenic atmosphere to ensure the prevention of reflow of the first insulating film even when the thermal oxidation is performed at higher temperatures.

As defined in Claim 29, a seventh process for fabrication of a semiconductor device functioning as a stacked DRAM cell comprises the steps of: depositing a lower interlayer insulating film on a semiconductor substrate, the lower interlayer insulating film having a property of reflowing due to a heat treatment under predetermined conditions; causing said lower interlayer insulating film to reflow for planarization thereof by the heat treatment; forming a contact hole extending through said lower interlayer insulating film to said impurity diffusion layer; depositing a polysilicon film on the whole surface of the substrate including said contact hole; patterning said polysilicon film to form a storage node and a contact connecting said storage node to said impurity diffusion layer; nitriding an exposed surface of said lower interlayer insulating film; depositing a silicon nitride film for a capacitor insulating film on the whole surface of the substrate including an exposed surface of said storage node, subsequently to the step of nitriding said lower interlayer insulating film; and thermally oxidizing the silicon nitride film for said capacitor insulating film to form an oxidized silicon nitride film.

According to this process, the initiation of nitriding can be speeded-up in laying a silicon nitride film over the lower interlayer insulating film, thus increasing the thickness of the resultant silicon nitride film for the capacitor insulating film. This is effective to

reduce the amount of oxygen penetrating the silicon nitride film during subsequent processes performed at elevated temperatures, thereby reducing tendency of the lower interlayer insulating film to reflow. Thus, a stacked DRAM cell having a capacitor insulating film free from wrinkle or cracks can be formed.

As defined in Claim 30, in the process of Claim 29, in the step of nitriding the surface of said lower interlayer insulating film, heat treatment may be performed in an atmosphere of nitrogen or ammonia.

As defined in Claim 31, an eighth process for fabrication of a semiconductor device functioning as a stacked DRAM cell comprises the steps of: depositing a lower interlayer insulating film made of a BPSG film on a semiconductor substrate, the lower interlayer insulating film having a property of not reflowing due to a heat treatment under predetermined conditions; causing said lower interlayer insulating film to reflow for planarization thereof by the heat treatment; forming a contact hole extending through said lower interlayer insulating film to said impurity diffusion layer; depositing a polysilicon film on the whole surface of the substrate including said contact hole; patterning said polysilicon film to form a storage node and a contact connecting said storage node to said impurity diffusion layer; depositing a silicon nitride film for a capacitor insulating film on the whole surface of the substrate including an exposed surface of said storage node; and thermally oxidizing the silicon nitride film for said capacitor insulating film to form an oxidized silicon nitride film.

According to this process, when heat treatment conditions during the oxidation of the oxidized silicon nitride film for the capacitor insulating film is set weaker than the predetermined conditions, the lower interlayer insulating film can be prevented from reflowing in the thermal oxidation step as soon as possible. Thus, a stacked DRAM cell can be formed which has a capacitor insulating film almost free from wrinkle or cracks.

As defined in Claim 32, in the process of Claim 31, the BPSG film may contain, as impurities, 5.0 wt% or less of phosphorus and 6.0 wt% or less of boron.

As defined in Claim 33, in the process of Claim 26, 29 or 31, a cylindrical storage node may be formed as said storage node.

[Embodiments of the Invention]

(Embodiment 1)

Fig. 1 is a sectional view partially showing a semiconductor device according to a first embodiment of the invention. For simplicity, Fig. 1 shows only a step at a gate but the semiconductor device of this embodiment includes a plurality of steps such as at a LOCOS isolation, gate and the like. The semiconductor device comprises a silicon substrate 1, a gate 2 as a first interconnection layer, a first BPSG film 3 (Boro-Phospho-silicate Glass) as a lower interlayer insulating film having a property of reflowing due to a heat treatment under predetermined conditions, a polycide interconnection 4 as a second interconnection layer comprising a lamination of a silicide film and a polysilicon film, a silicon oxide film 5 as a shape-holding film having a property of not reflowing due to a heat treatment under the aforesaid predetermined conditions causing the reflow of the first BPSG film, a silicon nitride film 6, and a second BPSG film 7 as an upper interlayer insulating film reflowable by a heat treatment under the aforesaid predetermined conditions.

Next, with reference to Figs. 2(A) to 2(D), description will be made on a method for fabrication of the semiconductor device with the structure shown in Fig. 1.

First, in a step shown in Fig. 2(A), the gate 2 is formed on the silicon substrate 1 and subsequently, the first BPSG film 3 is deposited on the whole surface of the substrate. At this time, the first BPSG film 3 contains phosphorus and boron as impurities in concentration of not less than 3.0 wt%, respectively. It is preferred that the first BPSG film 3 has a thickness more than double the thickness of the gate 2 because the first BPSG film 3 presents a better flatness as subjected to a heat treatment to be performed afterwards.

In a step shown in Fig. 2(B), a heat treatment is performed for planarizing the first BPSG film 3. The first BPSG film 3 can be planarized by heat treatment, for example, at 850°C in an atmosphere of nitrogen for 30 minutes. If the heat treatment is performed in an oxidation atmosphere, a like degree of flatness can be accomplished at a temperature of 800°C, provided that a nitride film as an antioxidation film must be laid under the first BPSG film 3.

Next, as shown in Fig. 2(C), the polycide interconnection 4 as the second interconnection layer is formed. Subsequently, the silicon oxide film 5 as the shape-holding film and the silicon nitride film 6 are deposited on the whole surface of the substrate. In this case, the silicon oxide film 5 has a thickness of 50 nm whereas the silicon nitride film 6 has a thickness of 50 nm. Incidentally, it is not necessarily required that the second interconnection layer be comprised of the polycide film. The second insulating film may comprise a polysilicon film or a silicide film as long as such a film sufficiently withstand a heat treatment for planarizing the first BPSG film 3.

In the subsequent step shown in Fig. 2(D), the second BPSG film 7 as an upper interlayer insulating film is deposited on the whole surface of the substrate. At this time, the second BPSG film 7 contains phosphorus and boron as impurities in concentration of not less than 3.0 wt%, respectively. The second BPSG film 7 preferably has a thickness more than double that of the polycide interconnection 4 because, as described above, the second BPSG film 7 presents a better flatness as subjected to a subsequent heat treatment. As deposited on the substrate, the second BPSG film 7 is subject to the heat treatment for planarization thereof. The second BPSG film 7 can be planarized by performing the heat treatment, for example, at 800°C in an oxidation atmosphere for 30 minutes. Thereafter, a normal process is performed wherein metallization of a desired pattern is provided and thus is completed the semiconductor device shown in Fig. 1.

According to this embodiment, even if the first BPSG film 3 already planarized reflows in the heat treatment for planarizing the second BPSG film 7, the silicon oxide film

5 not reflowable by the heat treatment at this temperature is interposed between the silicon nitride film 6 and the first BPSG film 3. Therefore, the embodiment of the invention assures the prevention of occurrence of wrinkle or cracks in the silicon nitride film 6. By virtue of the presence of the silicon nitride film 6 blocking oxygen penetration, the polycide interconnection 4 and the gate 2 are not oxidized even in the oxidation atmosphere and therefore, the heat treatment for film planarization may be performed in the oxidation atmosphere. More specifically, the heat treatment for film planarization may be performed at lower temperatures than the heat treatment in an atmosphere of nitrogen and hence, a semiconductor device featuring high performance and high reliability can be provided.

In this embodiment, the lower interlayer insulating film is comprised of the BPSG film containing phosphorus and boron in concentration of not less than 3.0 wt%, respectively, but it should be appreciated that the material for forming the lower interlayer insulating film should not be limited to this embodiment. Even where the lower interlayer insulating film is formed of another material presenting a similar degree of reflow in the heat treatment, interposing the silicon oxide film between the silicon nitride film and the lower interlayer insulating film provides a similar effect to this embodiment such that the occurrence of wrinkle or cracks in the silicon nitride film is prevented.

In this embodiment, it is important to define a thickness of the silicon oxide film 5 such that no cracks or wrinkle may occur in the silicon nitride film 6. A suitable value thereof is dependent upon a concentration of impurities in the first BPSG film 3 or a reflow temperature thereof, a thickness of the silicon nitride film 6 and conditions of the heat treatment subsequent to the formation of the silicon nitride film 6. As the concentration of the impurities in the first BPSG film 3 and the temperature of the heat treatment subsequent to the formation of the silicon nitride film 6 are decreased, or in other words, as the conditions have decreased tendency to cause the reflow of the first BPSG film 3, the thickness of the silicon oxide film 5 may be reduced. Conversely, as the conditions have

increased tendency to cause the reflow of the first BPSG film 3, the thickness of the silicon oxide film 5 must be increased. The greater the thickness of the silicon nitride film 6, the greater the stress produced in the silicon nitride film 6. Therefore, the silicon oxide film 5 is also required to have an increased thickness.

The thickness of the silicon nitride film 6 may be within a range such that the gate 2 or the polycide interconnection 4 at lower levels may not be oxidized during the heat treatment performed afterwards in the oxidation atmosphere.

According to this embodiment, although the shape-holding film interposed between the lower interlayer insulating film and the silicon nitride film is comprised of the silicon oxide film, it should be appreciated that the present invention is not limited to the above embodiment. The object of the invention may be achieved if the shape-holding film is formed of another material, provided that such a material is not caused to reflow by a heat treatment performed afterwards.

According to this embodiment, the heat treatment subsequent to the formation of the silicon nitride film is performed at 800°C in the oxidation atmosphere for 30 minutes. However, the effect of the invention can be attained by a heat treatment at a temperature lower than the above, provided that the conditions allow for the reflow of the lower interlayer insulating film. Incidentally, a heat treatment performed at higher temperatures provides a more conspicuous effect of the invention.

According to this embodiment, the lower interlayer insulating film defines a first interlayer insulating film on the semiconductor substrate, but the invention should not be limited to this. The invention is generally applicable to semiconductor devices such as of a multi-level interconnection structure wherein the lower interlayer insulating film may define a second or a third interlayer insulating film.

(Second Embodiment)

Fig. 3 is a sectional view showing a stacked DRAM cell as a semiconductor device in accordance with a second embodiment of the invention. In Fig. 3, the illustration of

the gate, LOCOS isolation and bit line is omitted for clarification of a portion featuring this embodiment. This semiconductor device comprises the silicon substrate 1, a BPSG film 8 as the first insulating film reflowable by a heat treatment under predetermined conditions, a silicon oxide film 9 as the shape-holding film which is not caused to reflow by a heat treatment under the aforesaid predetermined conditions, a contact 10 for connecting a storage node to an active region in the silicon substrate, a storage node 12, an oxidized silicon nitride film 14 serving as the capacitor insulating film, and a plate electrode 15.

Now, a process for fabrication of the semiconductor device shown in Fig. 3 will be described with reference to Figs. 4(A) and 4(B). In Figs. 4(A) and 4(B), as well, the illustration of the gate, LOCOS isolation and bit line is omitted for clarification of a portion featuring the embodiment.

In a step shown in Fig. 4(A), deposited on the silicon substrate 1 is the BPSG film 8 as the lower interlayer insulating film reflowable by a heat treatment under the predetermined conditions. At this time, the BPSG film 8 contains therein phosphorus and boron as impurities in concentration of not less than 3.0 wt%, respectively. Subsequently, a heat treatment is performed for planarization of the BPSG film 8, which may be planarized by heat treating, for example, at 850°C in an atmosphere of nitrogen for 30 minutes. Thereafter, deposited on the BPSG film 8 is the silicon oxide film 9 as the shape-holding film not reflowable by a heat treatment under the aforesaid predetermined conditions. Subsequent to opening a contact hole for storage node in the silicon oxide film 9 and the BPSG film 8, polysilicon is deposited on the whole surface of the substrate including the contact hole thereby forming the contact 10 and a polysilicon film 11 overlying the silicon oxide film 9. Normally, the polysilicon is added with N-type impurities.

In a step shown in Fig. 4(B), the polysilicon film 11 is etched into a desired pattern thereby forming the storage node 12. Subsequently, the silicon nitride film 13 is

deposited on the whole surface of the substrate in a thickness of about 8 nm.

The illustration of the subsequent steps is omitted. By oxidizing the aforesaid silicon nitride film 13, the oxidized silicon nitride film 14 shown in Fig. 3 is formed. The oxidation conditions at this time include, for example, a dry oxidation atmosphere, a temperature of 850°C and a processing time of 30 minutes. Thereafter, normal processes are performed to form the plate electrode 15 shown in Fig. 3 and then to metallize in a desired pattern whereby the semiconductor device is completed. In general practice, there are further overlaid an upper interlayer insulating film defining the second or third interlayer insulating film having a thermally reflowable property.

According to this embodiment, the silicon oxide film 9 not reflowable by a heat treatment under the predetermined conditions is interposed between the silicon nitride film 13 and the BPSG film 8, as shown in Fig. 4(B), and therefore, even if the thermal oxidation of the silicon nitride film 13 for forming the oxidized silicon nitride film 14 causes the BPSG film 8 to reflow, the resultant oxidized silicon nitride film 14 does not suffer the occurrence of wrinkle or cracks.

In this embodiment, the lower interlayer insulating film is comprised of the BPSG film containing phosphorus and boron in concentration of not less than 3.0 wt%, respectively, but it should be appreciated that a material for forming the lower interlayer insulating film is not limited to this. In case where the lower interlayer insulating film comprises another material presenting a similar degree of reflow in the heat treatment, as well, interposing the silicon oxide film between the silicon nitride film and the lower interlayer insulating film provides a similar effect to this embodiment such that the occurrence of wrinkle or cracks in the silicon nitride film is prevented.

In this embodiment, it is important to define a thickness of the silicon oxide film 9 such that no wrinkle or cracks may occur in the oxidized silicon nitride film 14. A suitable value thereof is dependent upon a concentration of impurities in the BPSG film 8, a thickness of the silicon nitride film 13 and conditions of the oxidation process subsequent

to the formation of the silicon nitride film 13. As the concentration of the impurities in the BPSG film 8 and the temperature of the oxidation process subsequent to the formation of the silicon nitride film 13 are decreased, or in other words, as the conditions have decreased tendency to cause the reflow of the BPSG film 8, the thickness of the silicon oxide film 5 may be reduced. Conversely, as the conditions have increased tendency to cause the reflow of the BPSG film 8, the thickness of the silicon oxide film 9 must be increased. The greater the thickness of the silicon nitride film 13, the greater the stress produced in the silicon nitride film 13 and therefore, the silicon oxide film 9 is also required to have an increased thickness.

The thickness of the silicon nitride film 13 may be within a range such that the underlying storage node 12 may not be oxidized during the subsequent oxidation process.

Although in this embodiment, the shape-holding film interposed between the lower interlayer insulating film and the silicon nitride film is comprised of the silicon oxide film, the present invention should not be limited to this. The object of the invention may be achieved if the shape-holding film is formed of another material, provided that such a material is not caused to reflow by a heat treatment performed afterwards under the predetermined conditions.

According to this embodiment, the silicon nitride film 13 is subject to the oxidation process at 850°C in a pyrogenic atmosphere for 30 minutes. However, the effect of the invention may be attained by an oxidation process performed at lower temperatures than this embodiment, provided that the oxidation conditions are such that the lower interlayer insulating film reflows. Incidentally, an oxidation process at higher temperatures provides a more conspicuous effect of the invention.

(Third Embodiment)

Fig. 5 is a sectional view showing a cylindrical stacked DRAM cell as a semiconductor device according to a third embodiment of the invention. In Fig. 5, the illustration of the gate, LOCOS isolation and bit line is omitted for clarification of a

portion featuring this embodiment. The semiconductor device comprises the silicon substrate 1, a BPSG film 16 as the lower interlayer insulating film reflowable by a heat treatment under predetermined conditions, a silicon oxide film 17 as the shape-holding film not reflowable by a heat treatment under the aforesaid predetermined conditions, a silicon nitride film 18 serving as a wet etching stopper film, a contact 19 for connecting a storage node to an active region in the silicon substrate, a cylindrical storage node 24, an oxidized silicon nitride film 23x functioning as the capacitor insulating film, and a plate electrode 25.

Now, a process for fabrication of the semiconductor device of Fig. 5 will be described with reference to Figs. 6(A) to 6(D). In Figs. 6(A) to 6(D), as well, the illustration of the gate, LOCOS isolation and bit line is omitted for clarification of a portion featuring this embodiment.

In a step shown in Fig. 6(A), deposited on the silicon substrate 1 is the BPSG film 16 as the lower interlayer insulating film reflowable by a heat treatment under the predetermined conditions. At this time, the BPSG film 16 contains therein phosphorus and boron as impurities in concentration of not less than 3.0 wt%, respectively. Subsequently, a heat treatment is performed for planarizing the BPSG film 16, which may be planarized by heat treating, for example, at 850°C in an atmosphere of nitrogen for 30 minutes. Thereafter, deposited on the BPSG film 16 is the silicon oxide film 17 as the shape-holding film not reflowable by a heat treatment under the predetermined conditions. Subsequently, there is formed the silicon nitride film 18 serving as the wet etching stopper in the formation of a cylindrical stacked cell. After opening a contact hole for storage node in the silicon nitride film 18, silicon oxide film 17 and BPSG film 16, polysilicon is deposited on the whole surface of the substrate including the contact hole so as to form the contact 19 and a polysilicon film 20 covering the silicon nitride film 18. Subsequently, a silicon oxide film 21 is laid over the polysilicon film 20.

In a step shown in Fig. 6(B), the silicon oxide film 21 is patterned into a desired cell configuration and then a polysilicon film 22 is deposited on the whole surface of the substrate. Prior to the deposition of the polysilicon film 22, native oxide formed on the polysilicon film 20 is removed.

In a step shown in Fig. 6(C), the polysilicon film 22 is subject to an anisotropic etching process such that the polysilicon film 22 is removed only except for a portion thereof on the side walls of the silicon oxide film 21 and thus is formed the cylindrical storage node 24.

In a step shown in Fig. 6(D), a wet etching process is performed by using the silicon nitride film 18 as the wet etching stopper thereby removing only the silicon oxide film 21. Subsequently, a silicon nitride film 23 is deposited on the whole surface of the substrate thereby covering therewith exposed surfaces of the silicon nitride film 18 and of the cylindrical storage node 24.

The illustration of the subsequent steps is omitted. By oxidizing the silicon nitride film 23, the oxidized silicon nitride film 23x of Fig. 5 is formed. Thereafter, normal processes are performed thereby forming the plate electrode 25 shown in Fig. 5 and then metallizing in a desired pattern whereby the semiconductor device is completed.

According to this embodiment, the silicon oxide film 17 not reflowable by a heat treatment under the predetermined conditions is interposed between the silicon nitride film 18 and the BPSG film 16 and therefore, neither the silicon nitride film 18 nor the oxidized silicon nitride film 23x suffers the occurrence of cracks or wrinkle therein even if the BPSG film 16 reflows during the thermal oxidation of the silicon nitride film 23 for forming the oxidized silicon nitride film 23x.

In this embodiment, the lower interlayer insulating film is comprised of the BPSG film containing phosphorus and boron in concentration of not smaller than 3 wt%, respectively, but it should be appreciated that a material for forming the lower interlayer insulating film is not limited to this. With a lower interlayer insulating film formed of

another material presenting a similar degree of reflow in the heat treatment, interposing the silicon oxide film between the silicon nitride film and the lower interlayer insulating film provides a similar effect to this embodiment such that the occurrence of wrinkle or cracks in the silicon nitride film 18 is prevented.

In this embodiment, it is important to define a thickness of the silicon oxide film 17 such that cracks or wrinkle may not occur in the silicon nitride film 18 or the oxidized silicon nitride film 23x. A suitable value thereof is dependent upon a concentration of the impurities in the BPSG film 16, a thickness of the silicon nitride film 18 and conditions of the oxidation process subsequent to the formation of the silicon nitride film 23. As the concentration of the impurities in the BPSG film 16 and the temperature of the oxidation process after the formation of the silicon nitride film 23 are decreased, or in other words, as the conditions have decreased tendency to cause the BPSG film 16 to reflow, the thickness of the silicon oxide film 17 may be reduced. Conversely, as the conditions have increased tendency to cause the BPSG film 16 to reflow, the thickness of the silicon oxide film 17 must be increased. Further, the greater the thicknesses of the silicon nitride film 18 and of the oxidized silicon nitride film 23x, the greater the stress produced in the silicon nitride film 18 and therefore, the thickness of the silicon oxide film 17 must be increased, as well.

The thickness of the silicon nitride film 18 may be in a range such that the underlying BPSG film 16 may not be attacked during the wet etch process performed afterwards.

In this embodiment, the shape-holding film interposed between the lower interlayer insulating film and the silicon nitride film is comprised of the silicon oxide film, but the present invention should not be limited to this. The object of the invention may be attained by the shape-holding film formed of another material, provided that such a material is not caused to reflow by a heat treatment performed afterwards under the predetermined conditions.

In the step shown in Fig. 6(B) wherein the silicon oxide film 21 is patterned into a desired cell configuration, a first modification of this embodiment may be adopted, comprising simultaneously etching the polysilicon film 20 along with the silicon oxide film, followed by depositing the polysilicon film 22 over the entire surface of the substrate, as shown in Fig. 7. Similarly to the above embodiment, this process is preferably preceded by the removal of the native oxide formed on the polysilicon film 20.

Further, a second modification of the embodiment may be adopted, wherein subsequent to the formation of the silicon nitride film 18 of Fig. 6(B) serving as the wet etching stopper, a silicon oxide film 27 is laid thereover. Next, with reference to Figs. 8(A) to 8(E), the second modification of the third embodiment will be described.

First, in a step shown in Fig. 8(A), deposited on the silicon substrate 1 is the BPSG film 16 as the lower interlayer insulating film, which is then subject to a heat treatment for planarization thereof. Thereafter, the silicon oxide film 17 and the silicon nitride film 18 as the wet etching stopper are laid thereover in the order named. Subsequent to further laying the silicon oxide film 27 over the silicon nitride film 18 , the contact hole for storage node is opened through the silicon oxide film 27, silicon nitride film 18, silicon oxide film 17 and BPSG film 16. Then, the polysilicon film is deposited on the whole surface of the substrate including the contact hole so as to form the contact 19 and the polysilicon film 20 over the silicon nitride film 27. Subsequently, the silicon oxide film 21 is deposited on the polysilicon film 20.

Similarly to the step of Fig. 6(B), a step shown in Fig. 8(B) comprises patterning the silicon oxide film 21 into a desired cell configuration, followed by depositing the polysilicon film 22 on the whole surface of the substrate. Prior to the deposition of the polysilicon film 22, the native oxide formed on the polysilicon film 20 is removed.

In a step shown in Fig. 8(C), the polysilicon film 22 is subject to an anisotropic etching process such that the polysilicon film 22 is removed only except for a portion

thereof on the side walls of the silicon oxide film 21 and thus is formed the cylindrical storage node 24.

In a step shown in Fig. 8(D), wet etching is performed by using the silicon nitride film 18 as the wet etching stopper thereby removing the silicon oxide films 21 and 27. In this state, a gap exists between the cylindrical storage node 24 and the silicon nitride film 18. Subsequently, the silicon nitride film 23 is deposited on the whole surface of the substrate thereby covering therewith exposed surfaces of the silicon nitride film 18 and of the cylindrical storage node 24.

In a step shown in Fig. 8(E), the silicon nitride film 23 is oxidized so as to form the oxidized silicon nitride film 23x. Thereafter, normal processes are performed thereby forming the plate electrode 25 and then metallizng in a desired pattern whereby the semiconductor device is completed.

In the case of the semiconductor device having a structure according to the modifications of the embodiment, the oxidized silicon nitride film 23x as the capacitor insulating film is formed for coverage over the surface of the cylindrical storage node 24 as well as that at the gap defined under a lower end thereof. Thus, the area of the cell is increased thereby accordingly increasing the capacity of the cell.

(Fourth Embodiment)

Next, description will be made on a structure of a stacked DRAM cell in accordance with a fourth embodiment of the invention wherein the nitride film is laid only under the plate electrode.

Fig. 9 is a sectional view showing a stacked DRAM cell as a semiconductor device according to the fourth embodiment of the invention. In Fig. 9, the illustration of the gate, LOCOS isolation and bit line is omitted for clarification of a portion featuring this embodiment. The semiconductor device comprises the silicon substrate 1, a first BPSG film 28 as the lower interlayer insulating film reflowable by a heat treatment under predetermined conditions, a contact 29 for connecting a storage node to the active region in

the substrate, a storage node 31, an oxidized silicon nitride film 33 functioning as the capacitor insulating film, a plate electrode 34, and a second BPSG film 35 as the upper interlayer insulating film reflowable by a heat treatment under the predetermined conditions.

Next, a process for fabrication of the semiconductor device of Fig. 9 will be described with reference to Figs. 10(A) and 10(B). It is to be noted here that in Figs. 10(A) and 10(B), the illustration of the gate, LOCOS isolation and bit line is omitted for clarification of a portion featuring this embodiment.

In a step shown in Fig. 10(A), deposited on the silicon substrate 1 is the first BPSG film 28 as the lower interlayer insulating film reflowable by a heat treatment under the predetermined conditions. At this time, the BPSG film 28 contains therein not more than 5.0 wt% of phosphorus and not more than 6.0 wt% of boron, as impurities. Subsequently, a heat treatment is performed for planarizing the first BPSG film 28, which may be planarized by heat treating, for example, at 850°C in an atmosphere of nitrogen for 30 minutes. After opening a contact hole for storage node, polysilicon is deposited on the whole surface of the substrate including the contact hole thereby forming the contact 29 filling the contact hole and the polysilicon film 30 over the first BPSG film 28. The polysilicon is normally added with N-type impurities.

In a step shown in Fig. 10(B), the polysilicon film 30 is etched into a desired pattern thereby to form the storage node 31. Subsequently, a silicon nitride film 32 is deposited on the whole surface of the substrate in a thickness of about 8 nm.

The illustration of the subsequent steps is omitted. The silicon nitride film 32 is oxidized for forming the oxidized silicon nitride film 33 shown in Fig. 9. At this time, the oxidation conditions include, for example, a dry oxidation atmosphere, a temperature of 800°C and a processing time of 30 minutes. Thereafter, a polysilicon film is laid over the whole surface of the substrate and etched into a desired pattern thereby to form the plate electrode 34. Concurrently with the etching of the plate electrode 34, the underlying

oxidized silicon nitride film 33 is removed at a portion corresponding to the removed portion of the plate electrode 34. Subsequently, deposited is the second BPSG film 35 as the upper interlayer insulating film which is reflowable by a heat treatment under the predetermined conditions. The second BPSG film 35 is planarized by heat treating, for example, at 850°C in the atmosphere of nitrogen for 30 minutes. Subsequently, the semiconductor device is completed by metallizing in a desired pattern.

According to the semiconductor device of this embodiment, when the heat treatment is performed for planarizing the second BPSG film 35, the oxidized silicon nitride film 33 does not exist except for a region underlying the plate electrode 34. That is, the top surface of the oxidized silicon nitride film 33 is covered with the plate electrode 34 formed of the polysilicon film. Accordingly, the oxidized silicon nitride film 35 is reinforced in terms of strength, and therefore the oxidized silicon nitride film 35 does not suffer the occurrence of wrinkle or cracks during the above heat treatment.

Further, according to this embodiment, when the silicon nitride film 32 is thermally oxidized to form the oxidized silicon nitride film 33, the plate electrode 34 is yet to exist and the silicon oxide film 9 such as provided in the second embodiment is not laid under the silicon nitride film 33. However, there occurs no wrinkle or cracks in the silicon nitride film 32 during this oxidation process because, unlike the second embodiment, the first BPSG film 28 contains the impurities in low concentration and the oxidation of the silicon nitride film 32 is performed at a relatively low temperature. The experiment conducted by the inventors demonstrates that if the first BPSG film 28 contains not more than 5.0 wt% of phosphorus and not more than 6.0 wt% of boron as the impurities, the dry oxidation of the silicon nitride film 32 can be accomplished at lower temperatures than the heat treatment for planarizing the first BPSG film 28 while preventing the occurrence of wrinkle or cracks in the silicon nitride film 32. It is to be noted that since the first BPSG film 28 contains the impurities in low concentration, the first BPSG film thus heat treated for planarization thereof presents a slightly lower flatness

than that of the second embodiment.

Fig. 11 is a sectional view showing a structure of a semiconductor device according to a modification directed to avoid the above drawback. According to this modification, the first BPSG film 28 contains the impurities in high concentration such that the film may be improved in flatness. Additionally, interposed between the first BPSG film 28 and the oxidized silicon nitride film 33 is the same silicon oxide film 9 with the second embodiment hereof that serves as the supporting film not reflowable by a heat treatment under the predetermined conditions. The presence of the silicon oxide film 9 is effective to prevent the occurrence of cracks or wrinkle in the silicon nitride film 32 even if the silicon nitride film 32 in the state shown in Fig. 10(B) is subject to the oxidation process. Incidentally, the semiconductor device of Fig. 11 has the same structure with the semiconductor device of Fig. 9 except for that the silicon oxide film 9 is provided.

As to the oxidation conditions for the silicon nitride film 32 affecting the reflow of the first BPSG film 28, the experiment demonstrates that the dry oxidation process presents a smaller tendency to produce reflow of the film than the pyrogenic oxidation process. It seems that this is because vapor penetrating the silicon nitride film 32 in the pyrogenic oxidation process presents a greater tendency to develop the reflow of the first BPSG film 28 than dry oxygen penetrating the silicon nitride film 32 in the dry oxidation process.

As to how the method of depositing the silicon nitride film 32 affects the resultant silicon nitride film, it is confirmed that more positive prevention of the occurrence of cracks or wrinkle is provided by subjecting the base to heat treatment (preprocess) in an atmosphere of nitrogen or ammonia prior to the deposition process. It seems that the preprocess performed in the atmosphere of nitrogen or ammonia provides a greater thickness of the resultant silicon nitride film 32 on the first BPSG film 28 than where the preprocess is not performed and therefore, the thicker silicon nitride film 32 reduces the amount of oxygen penetrating therethrough, resulting in harder reflow of the first BPSG film 28. The reason why the thickness of the silicon nitride film varies depending upon

whether the preprocess is performed or not is because difference in the state of the base varies the initiation of deposition process. The silicon nitride deposition on the BPSG film subject to no preprocessing presents a slower initiation of deposition than the silicon nitride deposition on the BPSG film preprocessed in the atmosphere of nitrogen.

(Fifth Embodiment)

Next, description will be made on a fifth embodiment of the invention wherein the DRAM cell structure of the fourth embodiment with the nitride film provided only beneath the plate electrode is applied to the cylindrical stacked DRAM cell structure.

Fig. 12 is a sectional view showing a cylindrical stacked DRAM cell as a semiconductor device according to the fifth embodiment of the invention. In Fig. 12, the illustration of the gate, LOCOS isolation and bit line is omitted for clarification of a portion featuring this embodiment. The semiconductor device comprises the silicon substrate 1, a first BPSG film 37 as the lower interlayer insulating film reflowable by a heat treatment under predetermined conditions, a silicon nitride film 38 serving as the wet etching stopper, a contact 39 for connecting a storage node to the active region in the silicon substrate, a cylindrical storage node 44, an oxidized silicon nitride film 43x serving as the capacitor insulating film, a plate electrode 45, and a second BPSG film 46 reflowable by a heat treatment under the predetermined conditions.

Now, a process for fabrication of the semiconductor device shown in Fig. 12 will be described with reference to Figs. 13(A) to 13(D). It is to be noted here that Figs. 13(A) to 13(D) omit the illustration of the gate, LOCOS isolation and bit line for clarification of the portion featuring this embodiment.

First in a step shown in Fig. 13(A), deposited on the silicon substrate 1 is the first BPSG film 37 as the lower interlayer insulating film reflowable by a heat treatment under the predetermined conditions. At this time, the first BPSG film 37 contains therein not more than 5.0 wt% of phosphorus and not more than 6.0 wt% of boron as impurities.

Subsequently, the first BPSG film 37 is subject to a heat treatment for planarization thereof. The first BPSG film 37 may be planarized by heat treating, for example, at 850°C in an atmosphere of nitrogen for 30 minutes. Next, the silicon nitride film 38 is formed, which serves as the wet etching stopper during the formation of the cylindrical stacked cell. After opening a contact hole in the silicon nitride film 38 and the first BPSG film 37, polysilicon is deposited on the whole surface of the substrate including the contact hole thereby forming the contact 39 and a polysilicon film 40 over the silicon nitride film 38. Subsequently, a silicon oxide film 41 is laid over the polysilicon film 40.

In a step shown in Fig. 13(B), the silicon oxide film 41 is patterned into a desired cell configuration and then, a polysilicon film 42 is deposited on the whole surface of the substrate. Incidentally, the native oxide formed on the polysilicon film 40 is removed prior to the deposition of the polysilicon film 42.

In a step shown in Fig. 13(C), the polysilicon film 42 is subject to the anisotropic etching such that the polysilicon film 22 is removed only except for a portion thereof on the side walls of the silicon oxide film 41 and thus is formed the cylindrical storage node 44.

In a step shown in Fig. 13(D), a wet etching process is performed by using the silicon nitride film 38 as the wet etching stopper, thereby removing only the silicon oxide film 41. Subsequently, a silicon nitride film 43 is deposited on the whole surface of the substrate in a thickness of about 8 nm thereby covering exposed surfaces of the silicon nitride film 38 and the cylindrical storage node 44 therewith.

The illustration of the subsequent steps is omitted. The oxidized silicon nitride film 43x shown in Fig. 12 is formed by oxidizing the silicon nitride film 43. The oxidation conditions therefor include, for example, a pyrogenic atmosphere, a temperature of 800°C and a processing time of 30 minutes. Subsequently, a polysilicon film is deposited on the whole surface of the substrate and etched into a desired pattern thereby to form the plate electrode shown in Fig. 12. Concurrently with the etching of the plate

electrode 45, the underlying oxidized silicon nitride film 43x and the silicon nitride film 38 as the wet etching stopper are removed at a region except for a region corresponding to the plate electrode 45. Thereafter, the second BPSG film 46 as the upper interlayer insulating film shown in Fig. 12 is deposited and then planarized by heat treatment which is performed, for example, at 850°C in the atmosphere of nitrogen for 30 minutes. The semiconductor device is completed by metallizing in a desired pattern.

According to the semiconductor device of this embodiment, similarly to the fourth embodiment of the invention, the heat treatment for planarization of the second BPSG film 46 does not result in the occurrence of wrinkle or cracks in the silicon nitride film 38 nor the oxidized silicon nitride film 43x because the oxidized silicon nitride film 43s and the silicon nitride film 38 as the wet etching stopper are absent in the region except for that lying under the plate electrode 45.

In this embodiment, when the silicon nitride film 43 is thermally oxidized to form the oxidized silicon nitride film 43x, the plate electrode 45 is yet to exist and the silicon oxide film 17 such as provided in the third embodiment is not provided under the silicon nitride film 43 nor the silicon nitride film 38. However, this oxidation process does not entail the occurrence of wrinkle or cracks in the silicon nitride film 38 nor in the oxidized silicon nitride film 43x. This is because unlike the aforementioned third embodiment, the first BPSG film 37 contains the impurities in low concentration and the thermal oxidation of the silicon nitride film 43 is performed at a relatively low temperature.

Incidentally, where for the purpose of improving the flatness of the first BPSG film 37, for example, the thermal oxidation of the silicon nitride film 43 must be performed under such conditions as to cause the reflow of the first BPSG film 37, a silicon oxide film may be laid under the silicon nitride film 38.

Fig. 14 is a sectional view showing a structure of a semiconductor device according to such a modification of the embodiment. According to this modification, the first BPSG film 37 contains the impurities in higher concentration for improvement of the

flatness thereof while interposed between the first BPSG film 37 and the silicon nitride film 38 is the same silicon oxide film 17 as in the third embodiment, the film serving as the shape-holding film not reflowable by a heat treatment under the predetermined conditions. The presence of this silicon oxide film 17 is effective to prevent the occurrence of cracks or wrinkle in the silicon nitride film 38 and the oxidized silicon nitride film 43x even if the oxidation of the silicon nitride film 43 is performed in the state shown in Fig. 13(D). Incidentally, the semiconductor device of Fig. 14 has the same structure as the aforementioned semiconductor device of in Fig. 12 except for that the silicon oxide film 17 is provided. According to this modification, the addition of the silicon oxide film 17 provides a more stable fabrication process.

(Modifications of the Foregoing Embodiments)

In the foregoing second to fifth embodiments, if a film having a high etching selectivity to the oxide film is first deposited on the whole surface of the substrate and then the contact hole is opened, the etched contact hole is prevented from increasing in size.

Figs. 15(A) and 15(B) illustrate the step to form the contact hole in the fabrication process according to the second embodiment, showing difference in the shape of the contact hole between a case where a polysilicon film 47 as an edge retaining film having a high etching selectivity to the oxide film is provided and a case where no polysilicon film is provided (second embodiment). As seen in Fig. 15(A), where the polysilicon film 47 having a high etching selectivity to the oxide film is laid over the silicon oxide film 9, the presence of the polysilicon film 47 is effective to prevent the expansion of an upper portion of the contact hole, as shown in Fig. 15(B), regardless of variations of the etching conditions.

In the foregoing embodiments, the interlayer insulating film having the property of reflowing due to a heat treatment under the predetermined conditions is comprised of the BPSG film, but the present invention should not be limited to these embodiments. Obviously, the invention is applicable to insulating films such as added with arsenic

instead of phosphorus, and as further added with fluorine for imparting a property of reflowing due to a heat treatment at further reduced temperatures.

According to the foregoing embodiments, the shape-holding film is interposed between the lower interlayer insulating film and the silicon nitride film, but the present invention should not be limited to these embodiments. For example, with the shape-holding film such as of the silicon oxide film or the like interposed between the silicon nitride film and the upper interlayer insulating film, the process for planarizing the upper interlayer insulating film or the like ensures the prevention of occurrence of wrinkle or cracks in the silicon nitride film.

According to the above embodiments pertaining the DRAM cells, all the first insulating films define a so-called first interlayer insulating film directly laid over the substrate, but the present invention should not be limited to these embodiments. In some type of the DRAM cells, the storage node may be formed on the second interlayer insulating film or on an interlayer insulating film at a further upper level. In such a case, the lower interlayer insulating film denotes an interlayer insulating film immediately under the storage node or all the interlayer insulating films thereunder.

[Effects of the Invention]

In a semiconductor device of the present invention comprising an insulating film having a property of reflowing due to heat treatment under predetermined conditions and an insulating film containing at least silicon nitride and a process for fabrication of the same, a shape-holding film is formed on at least one of the top of the upper surface and bottom of the lower surface of the insulating film containing silicon nitride. Therefore, even if the heat treatment or the like causes the first insulating film to reflow, the second insulating film is supported by the shape-holding film. Thus, the second insulating film does not suffer the occurrence of wrinkle or cracks therein. This leads to an enhanced yield, reliability and performance of the semiconductor devices.

When the semiconductor device is a stacked DRAM cell comprising a capacitor

insulating film made of an oxidized silicon nitride film, a shape-holding film is provided between a lower interlayer insulating film and a film containing silicon nitride or a plate electrode is allowed to function as the shape-holding film. This can prevent the capacitor insulating film from suffering the occurrence of wrinkle or cracks therein during a step of oxidizing a silicon nitride film for a capacitor insulating film and a step of planarizing an upper interlayer insulating film. This leads to an enhanced yield, reliability and performance of the semiconductor devices functioning as stacked DRAM cells.

Furthermore, when the semiconductor device is a cylindrical stacked DRAM cell comprising a capacitor insulating film made of an oxidized silicon nitride film and a silicon nitride film for an etching stopper, the similar countermeasure as described above can prevent the capacitor insulating film and a silicon oxide film for an etching stopper from suffering the occurrence of wrinkle or cracks therein during a step of oxidizing a silicon nitride film for a capacitor insulating film and a step of planarizing an upper interlayer insulating film. This leads to an enhanced yield, reliability and performance of the semiconductor devices functioning as cylindrical stacked DRAM cells.

[Brief Description of the Drawings]

[Fig. 1]

Fig. 1 is a sectional view showing a structure of a semiconductor device having a polycide interconnection in accordance with a first embodiment of the invention.

[Fig. 2]

Figs. 2 are sectional views for illustrating steps for fabricating the semiconductor device according to the first embodiment hereof.

[Fig. 3]

Fig. 3 is a sectional view showing a structure of a stacked DRAM cell in accordance with a second embodiment of the invention.

[Fig. 4]

Figs. 4 are sectional views for illustrating steps for fabricating the semiconductor

device according to the second embodiment hereof.

[Fig. 5]

Fig. 5 is a sectional view showing a structure of a cylindrical stacked DRAM cell in accordance with a third embodiment of the invention.

[Fig. 6]

Figs. 6 are sectional views for illustrating steps for fabricating the cylindrical stacked DRAM cell according to the third embodiment hereof.

[Fig. 7]

Fig. 7 is a sectional view for illustrating only one of the steps for fabricating a cylindrical stacked DRAM cell according to a first modification of the third embodiment hereof.

[Fig. 8]

Figs. 8 are sectional views for illustrating steps for fabricating a cylindrical stacked DRAM cell according to a second modification of the third embodiment hereof.

[Fig. 9]

Fig. 9 is a sectional view showing a structure of a stacked DRAM cell in accordance with a fourth embodiment of the invention.

[Fig. 10]

Fig. 10 are sectional views for illustrating steps for fabricating the stacked DRAM cell according to the fourth embodiment hereof.

[Fig. 11]

Fig. 11 is a sectional view showing a structure of a stacked DRAM cell according to a modification of the fourth embodiment hereof.

[Fig. 12]

Fig. 12 is a sectional view showing a structure of a cylindrical stacked DRAM cell in accordance with a fifth embodiment of the invention.

[Fig. 13]

Figs. 13 are sectional views for illustrating steps for fabricating the cylindrical stacked DRAM cell according to the fifth embodiment hereof.

[Fig. 14]

Fig. 14 is a sectional view showing a structure of a cylindrical stacked DRAM cell according to a modification of the fifth embodiment hereof.

[Fig. 15]

Figs. 15 are sectional views for illustrating a modification of another embodiment of the invention directed to the prevention of a size increase of a contact hole.

[Fig. 16]

Fig. 16 is a sectional view showing a structure of a prior-art semiconductor device having a polycide interconnection.

[Fig. 17]

Fig. 17 is a sectional view showing a structure of a prior-art stacked DRAM cell.

[Fig. 18]

Fig. 18 is a sectional view showing a structure of a cylindrical stacked DRAM cell known to the art.

[Fig. 19]

Figs. 19 are sectional views each illustrating a state in which wrinkle or crack is produced in the silicon nitride film of the prior-art semiconductor device.

[Name of the Document] ABSTRACT

[Summary]

[Purpose] A semiconductor device free from wrinkle or cracks in the nitride film associated with thermal history and a process for fabrication of the same can be offered, even though the nitride film is laid over the insulating film having a reflowable property.

[Solution] A DRAM cell transistor formed on a silicon substrate 1 comprises a BPSG film 8, a silicon oxide film 9 as a shape-holding film laid thereover, a contact 10 filling a contact hole extended through the silicon oxide film 9 and the BPSG film 8, a storage node 12, an oxidized silicon nitride film 14 as a capacitor insulating film, and a plate electrode 15. There may be further provided a second BPSG film thereover. Even if the BPSG film 8 is caused to reflow by a process for oxidizing the silicon nitride film for formation of the oxidized silicon nitride film as the capacitor insulating film, the silicon oxide film as the silicon nitride film is supported by the silicon oxide film 9, and hence, the oxidized silicon nitride film free from wrinkle or cracks is provided.

[Selected Figure] Fig.3

[Name of the Document] DRAWINGS

Fig. 1

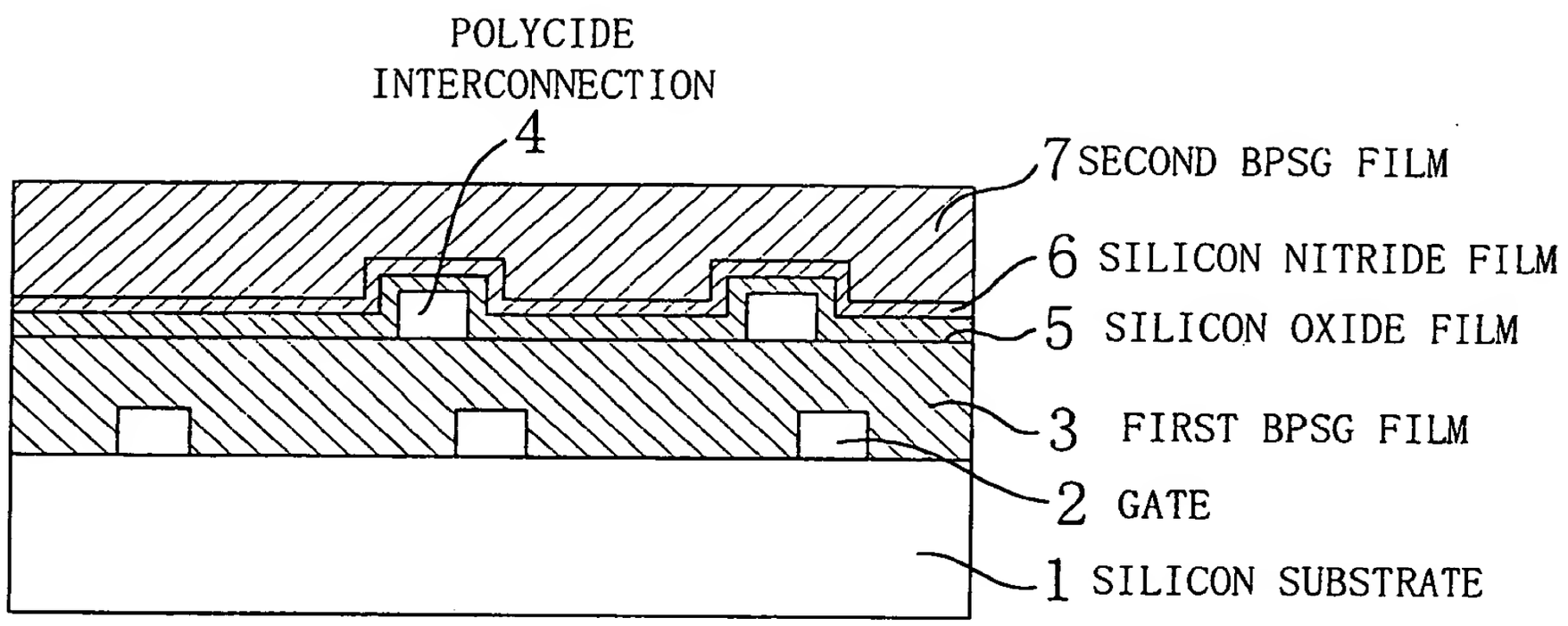

Fig. 2(A)

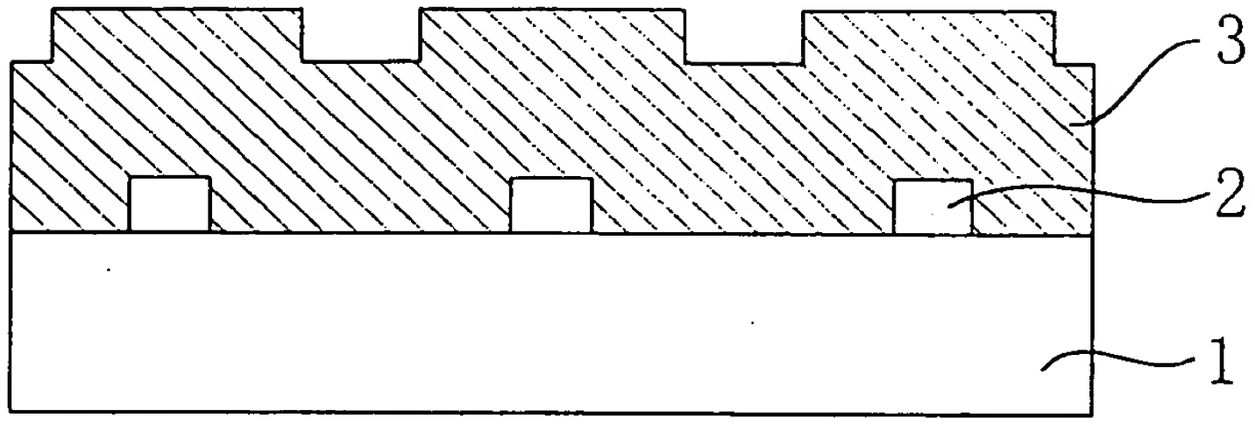

Fig. 2(B)

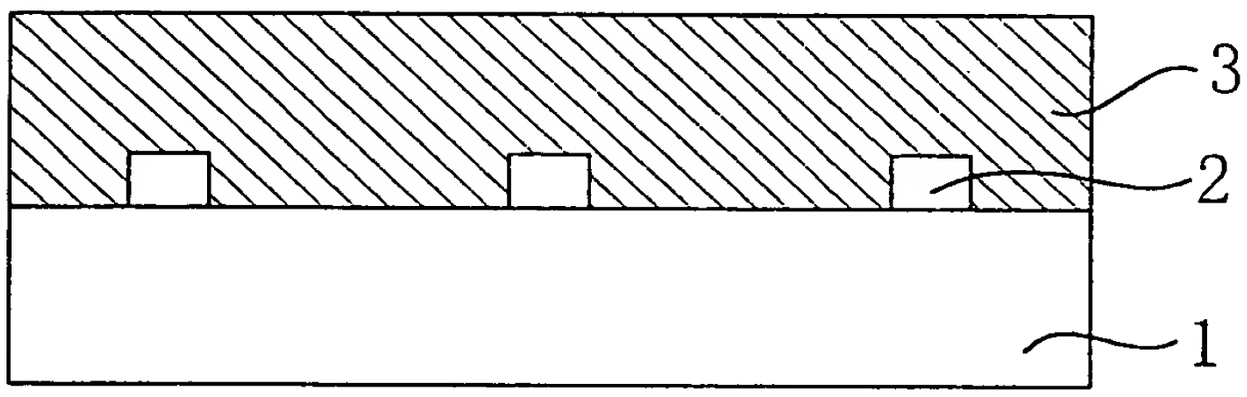

Fig. 2(C)

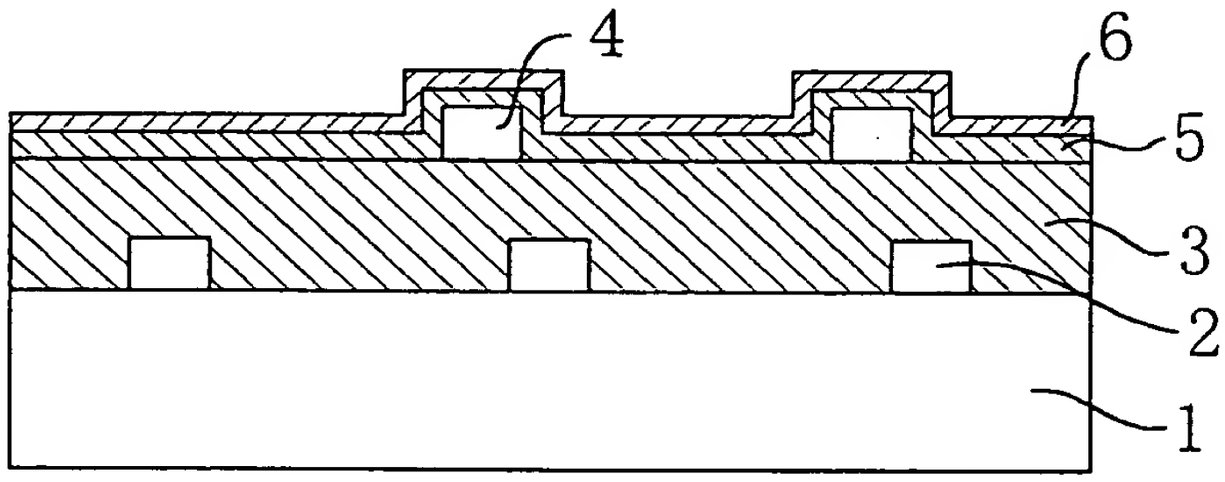

Fig. 2(D)

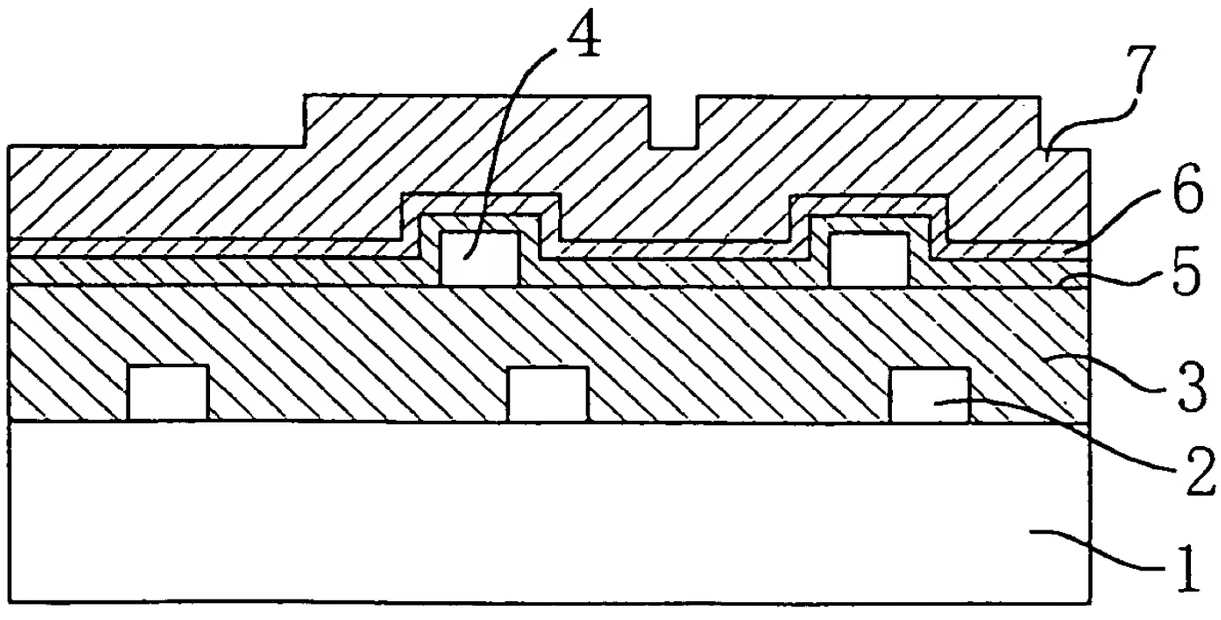

Fig. 3

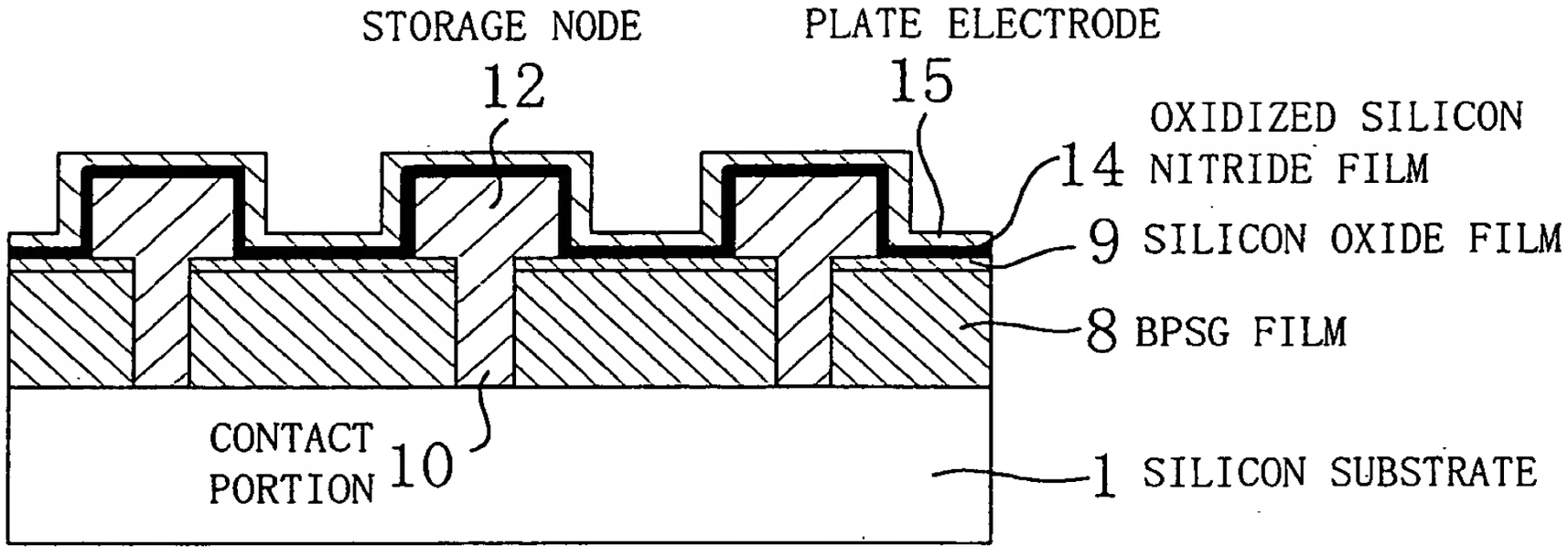
STORAGE NODE
12
PLATE ELECTRODE
15
OXIDIZED SILICON
14 NITRIDE FILM
9 SILICON OXIDE FILM
8 BPSG FILM
CONTACT
PORTION 10
1 SILICON SUBSTRATE

Fig. 4(A)

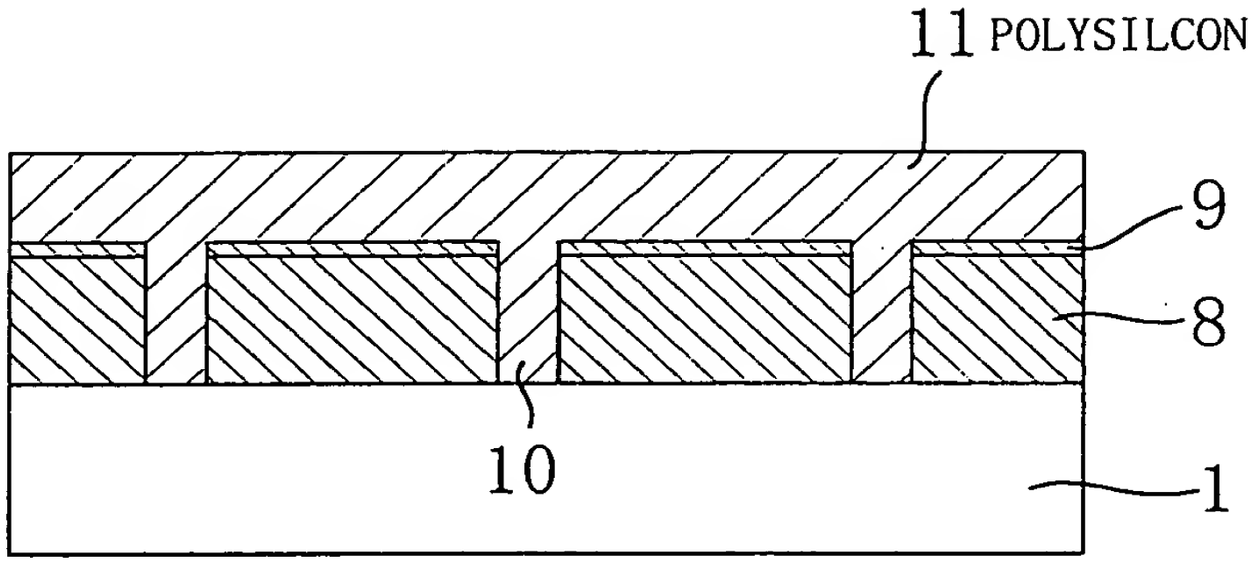

Fig. 4(B)

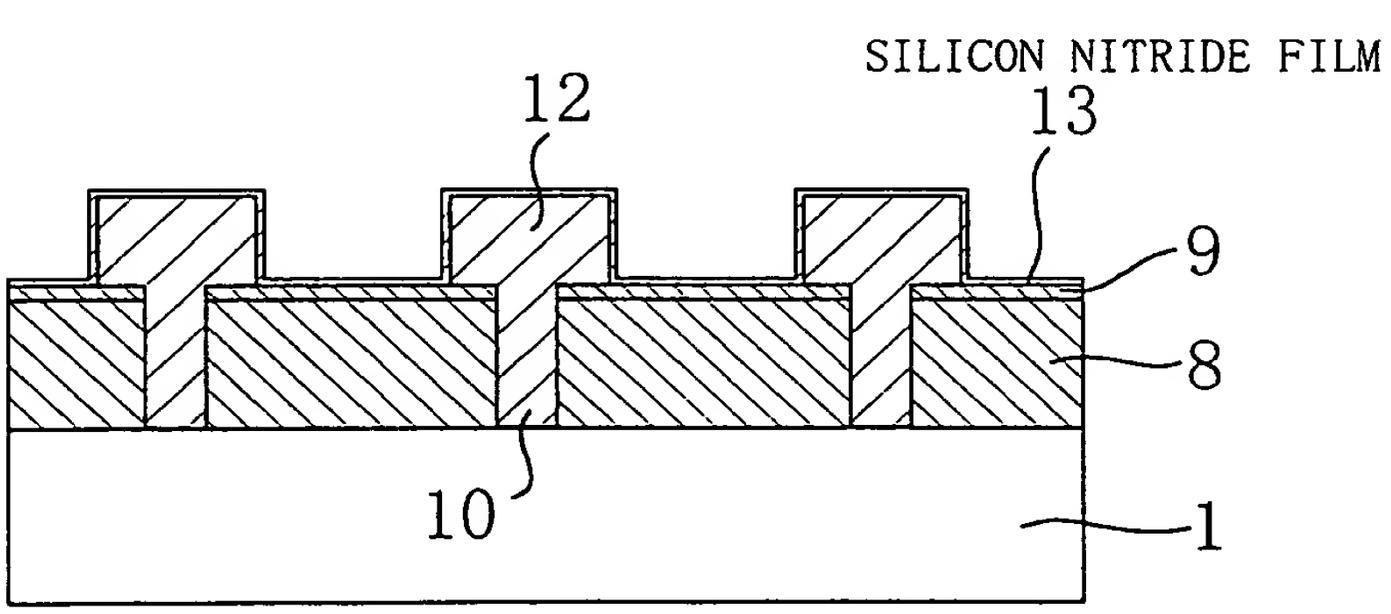

Fig. 5

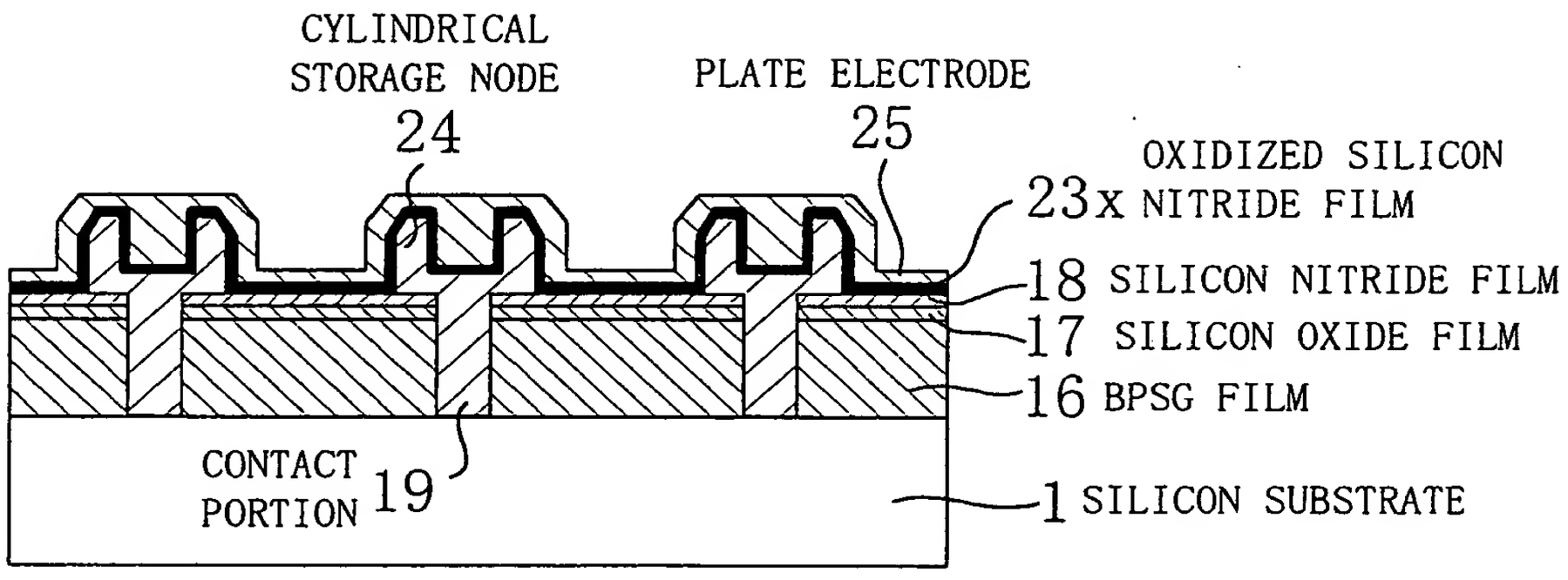
CYLINDRICAL
STORAGE NODE
24
PLATE ELECTRODE
25
OXIDIZED SILICON
23x NITRIDE FILM
18 SILICON NITRIDE FILM
17 SILICON OXIDE FILM
16 BPSG FILM
CONTACT
PORTION 19
1 SILICON SUBSTRATE

Fig. 6(A)

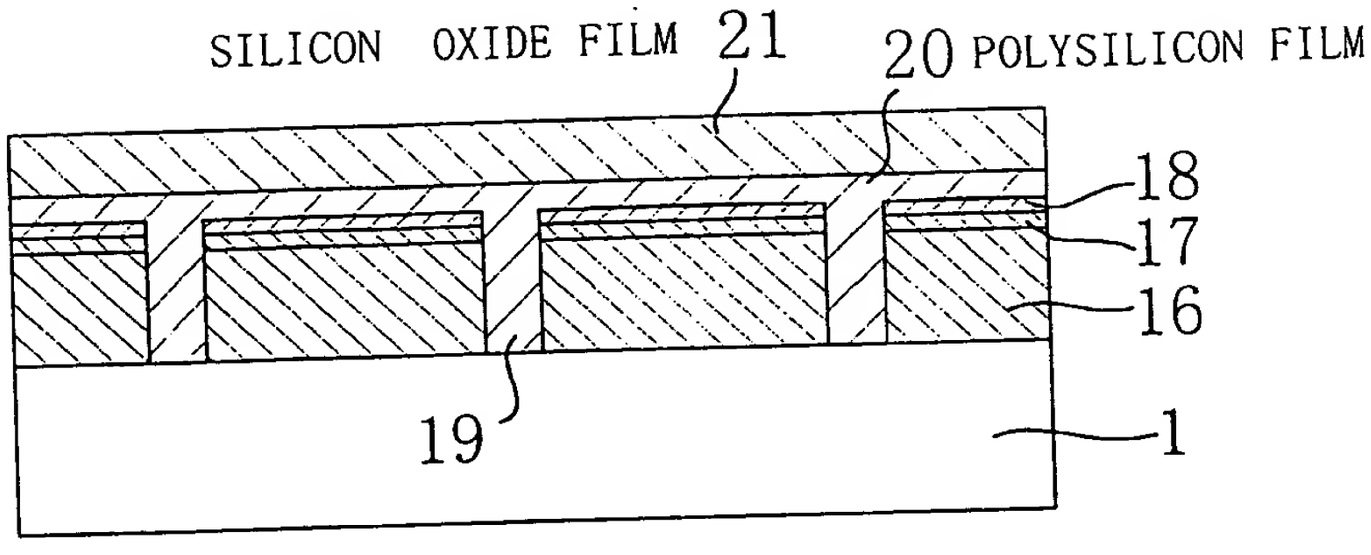

Fig. 6(B)

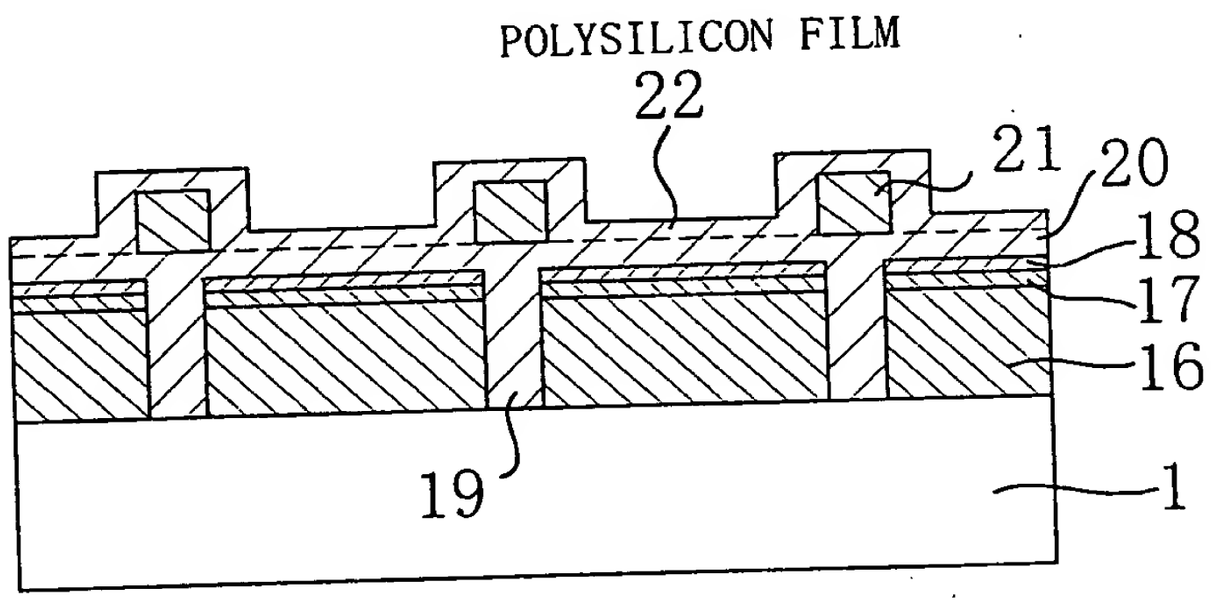

Fig. 6(C)

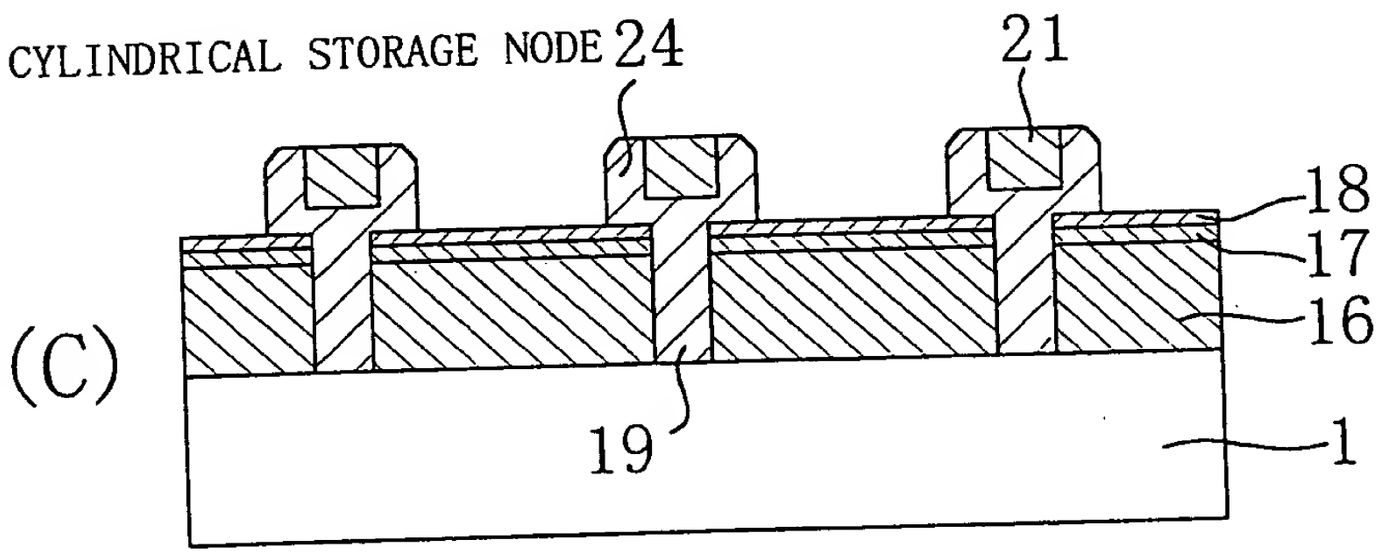

Fig. 6(D)

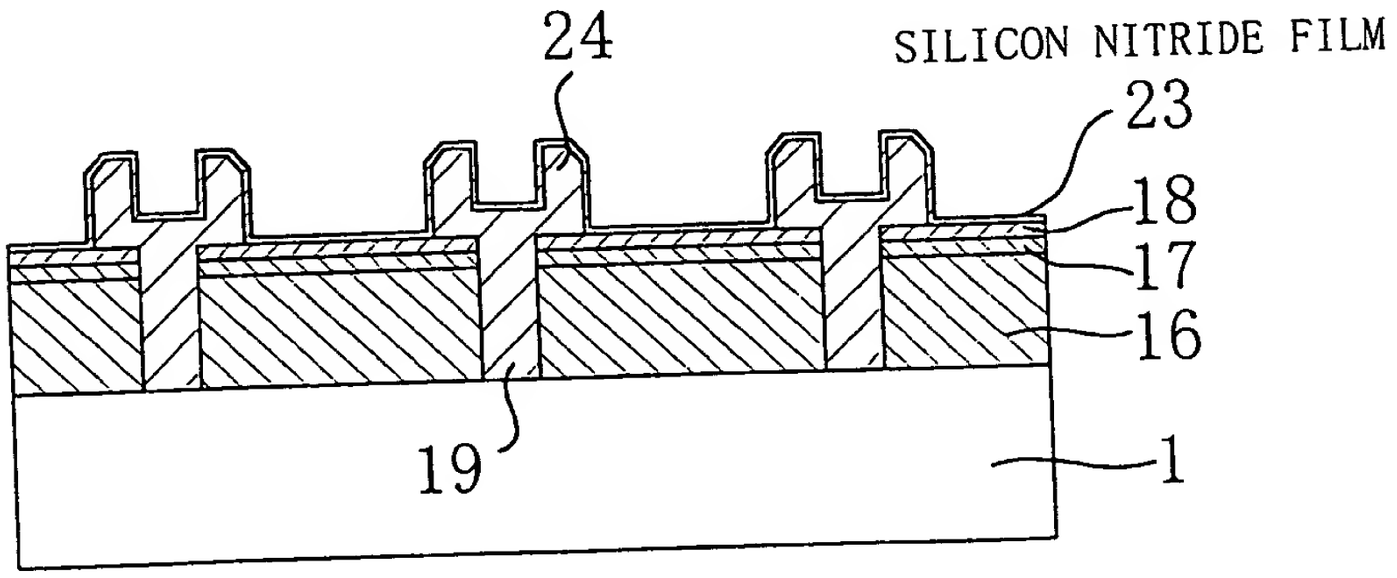

Fig. 7

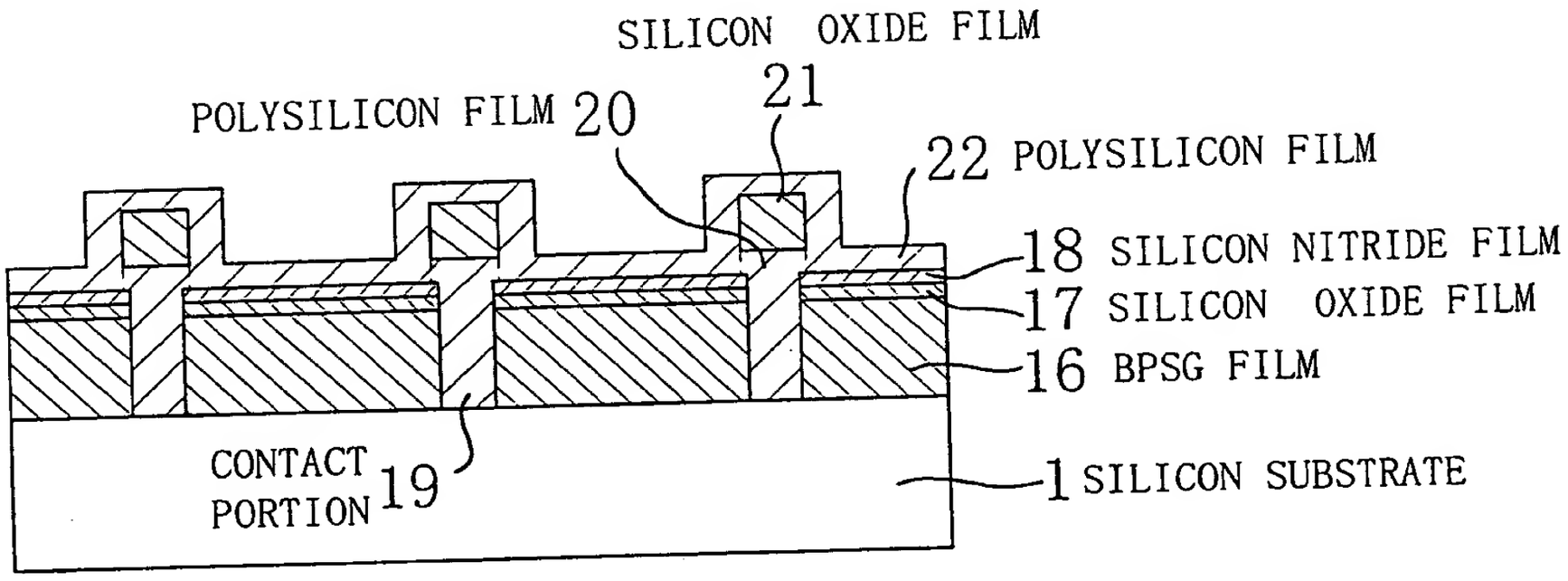
SILICON OXIDE FILM
POLYSILICON FILM
20
21
22 POLYSILICON FILM
18 SILICON NITRIDE FILM
17 SILICON OXIDE FILM
16 BPSG FILM
CONTACT PORTION
19
1 SILICON SUBSTRATE

Fig. 8(A)

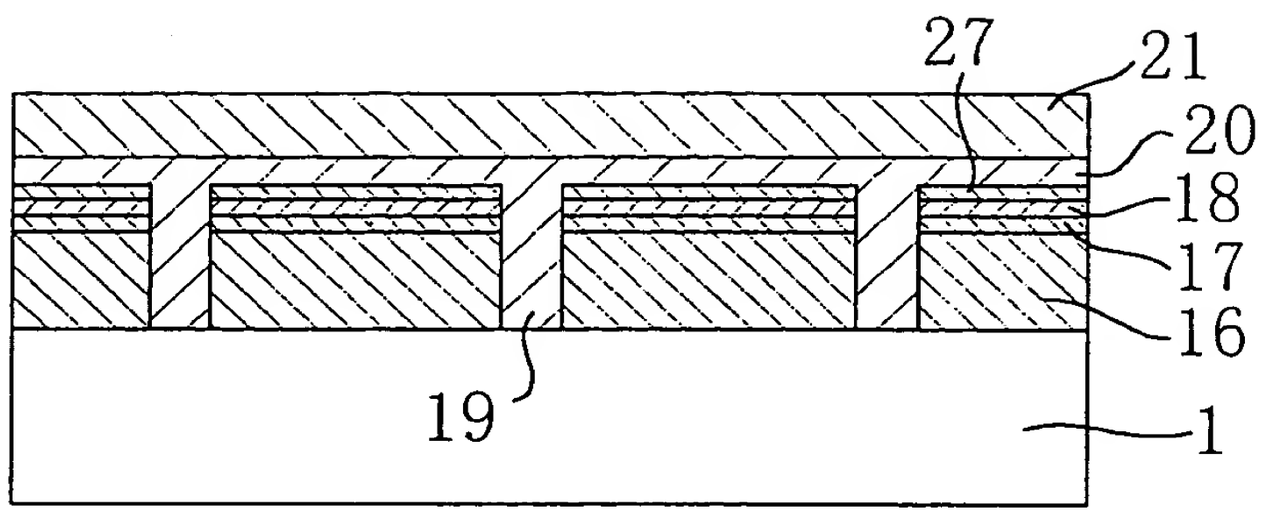

Fig. 8(B)

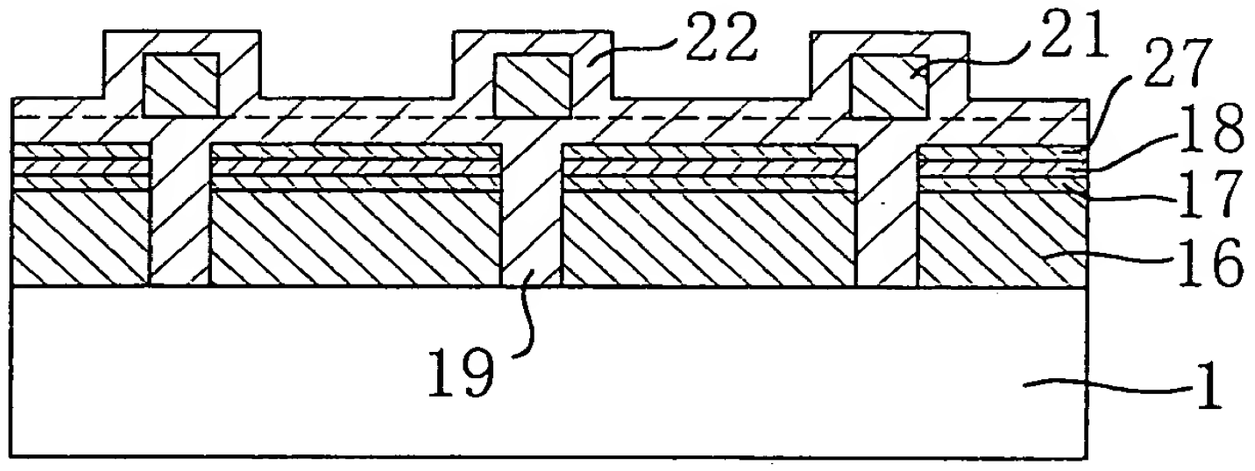

Fig. 8(C)

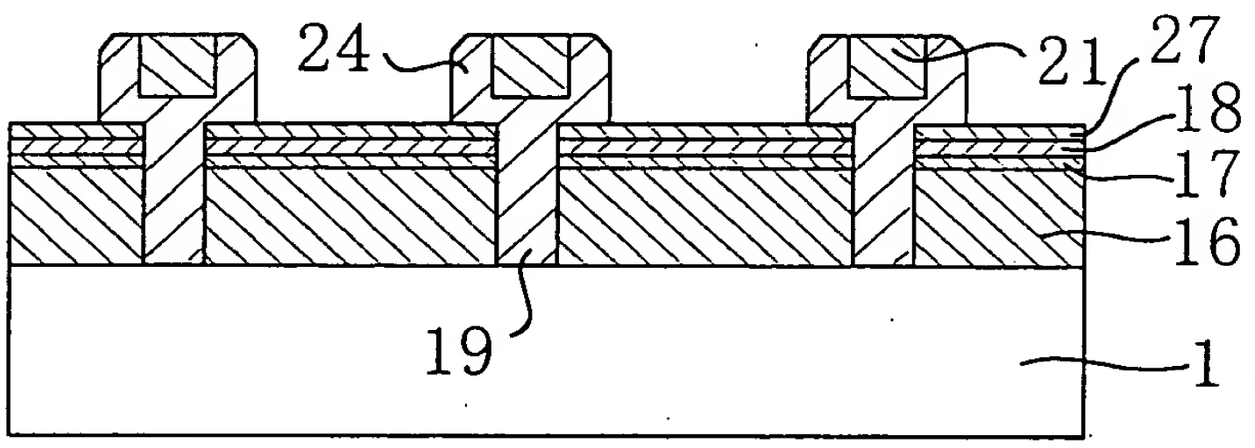

Fig. 8(D)

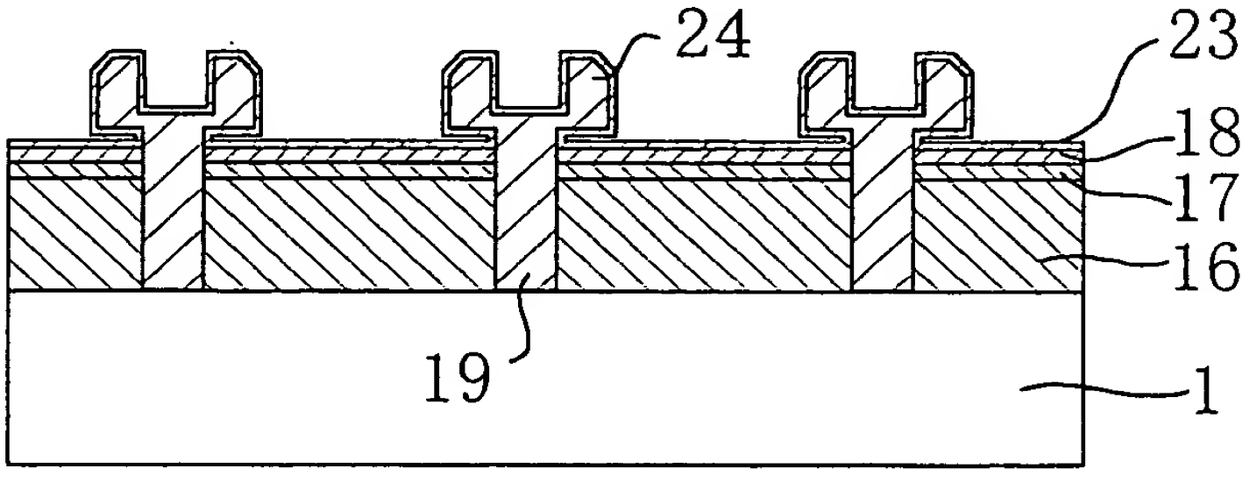

Fig. 8(E)

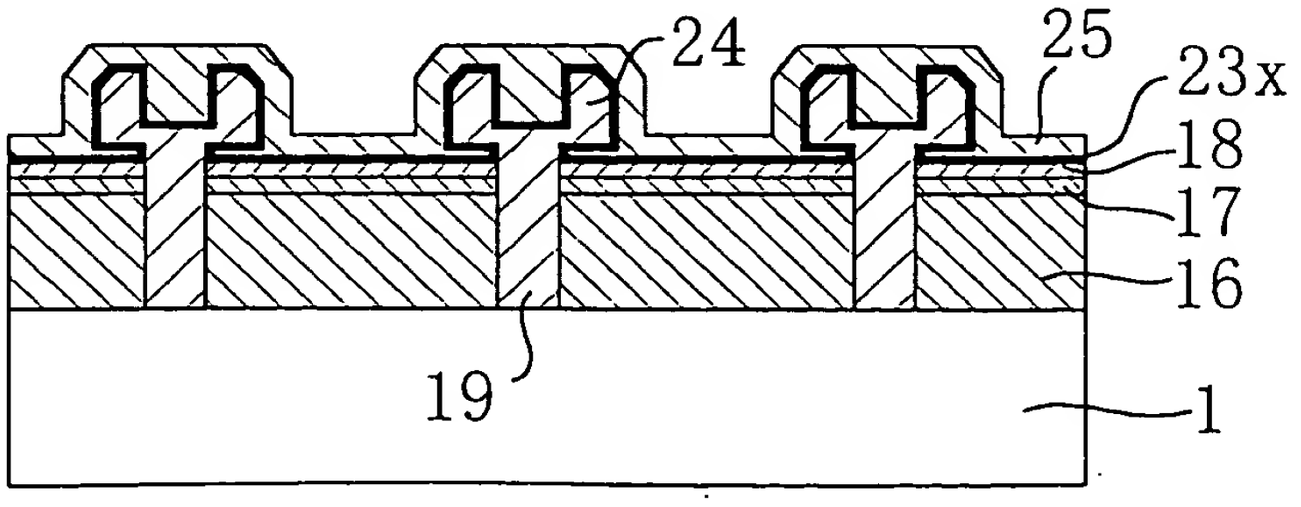

Fig. 9

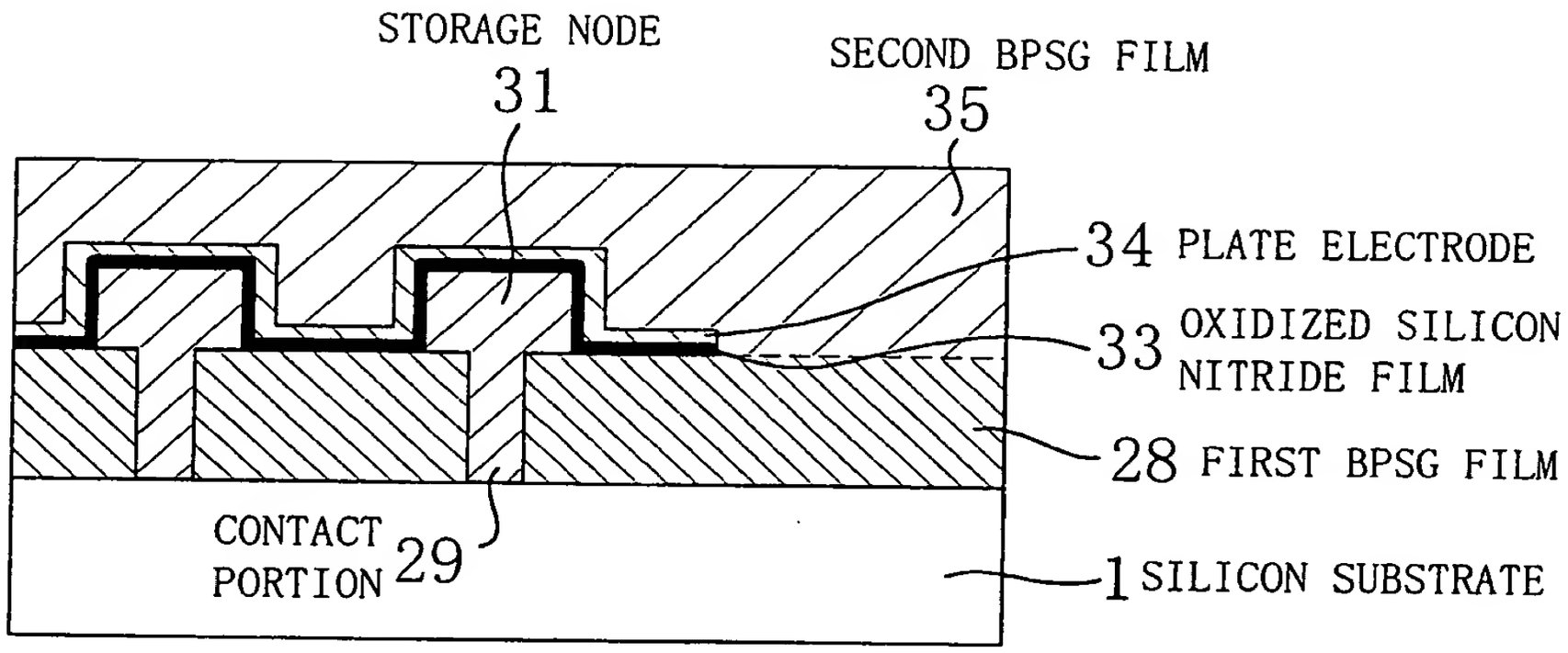
STORAGE NODE
31
SECOND BPSG FILM
35
34 PLATE ELECTRODE
33 OXIDIZED SILICON NITRIDE FILM
28 FIRST BPSG FILM
CONTACT PORTION 29
1 SILICON SUBSTRATE

Fig. 10(A)

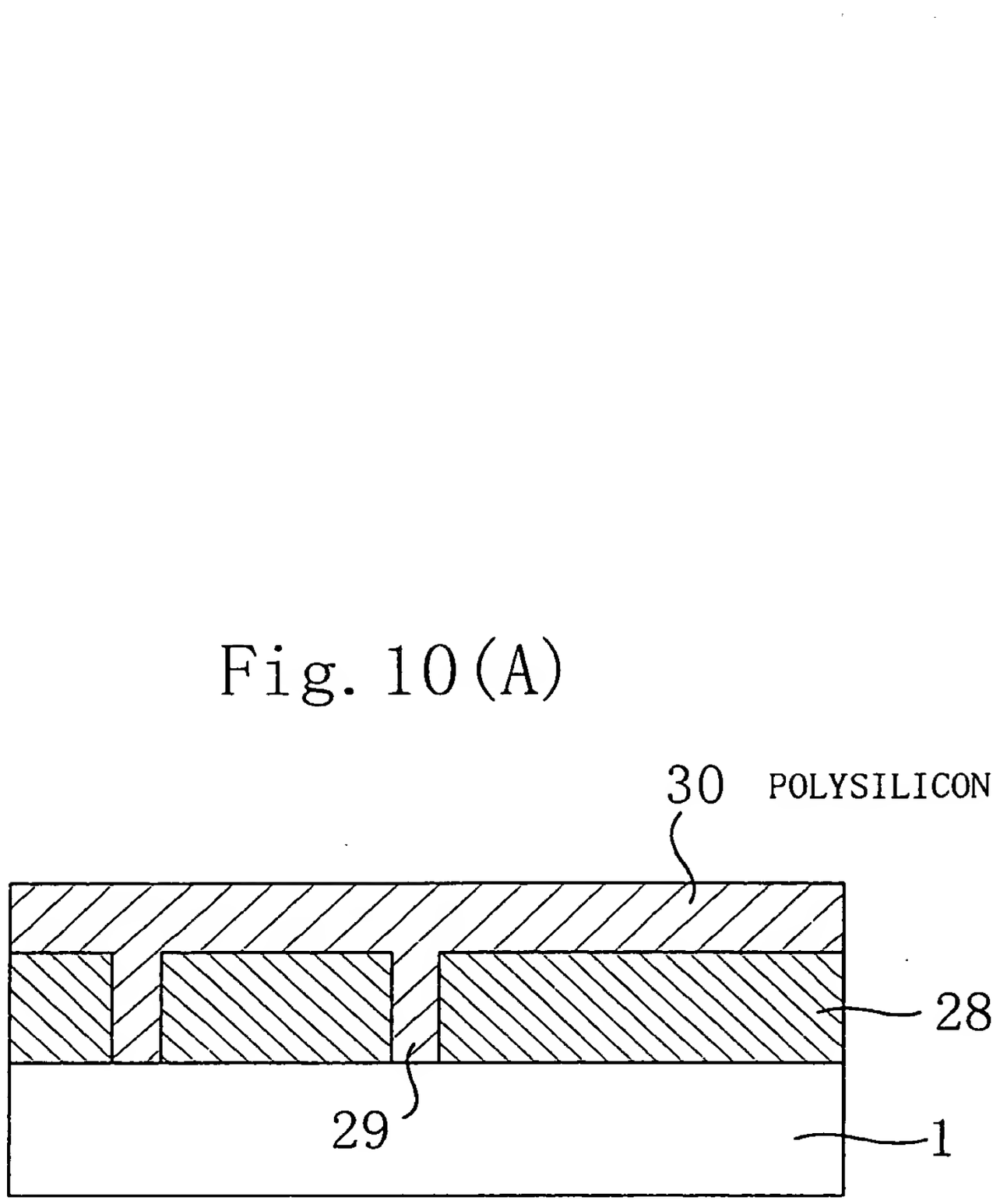

Fig. 10(B)

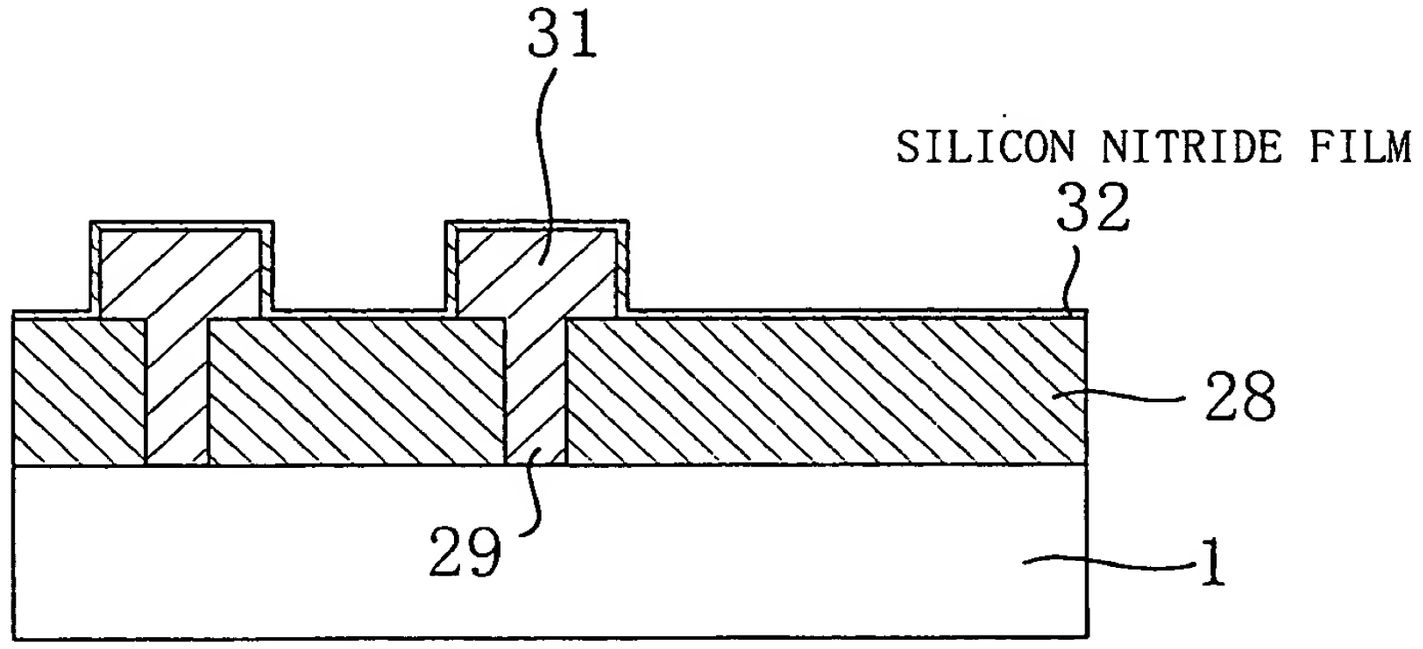

Fig. 11

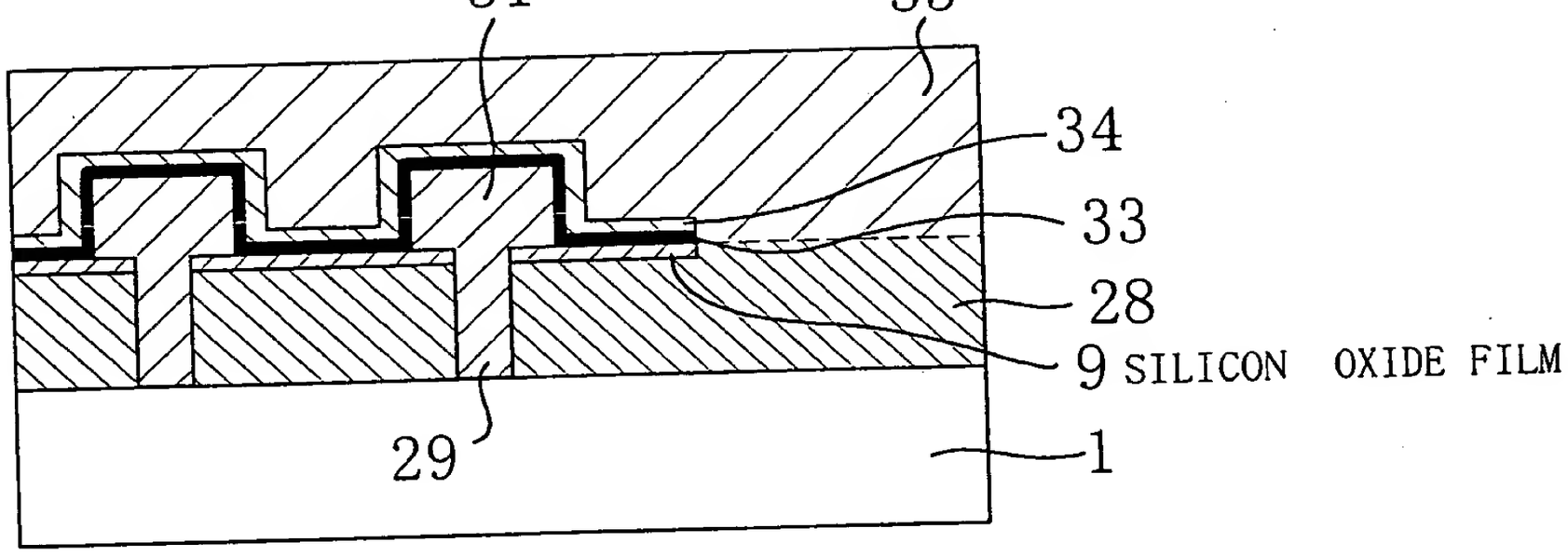

Fig. 12

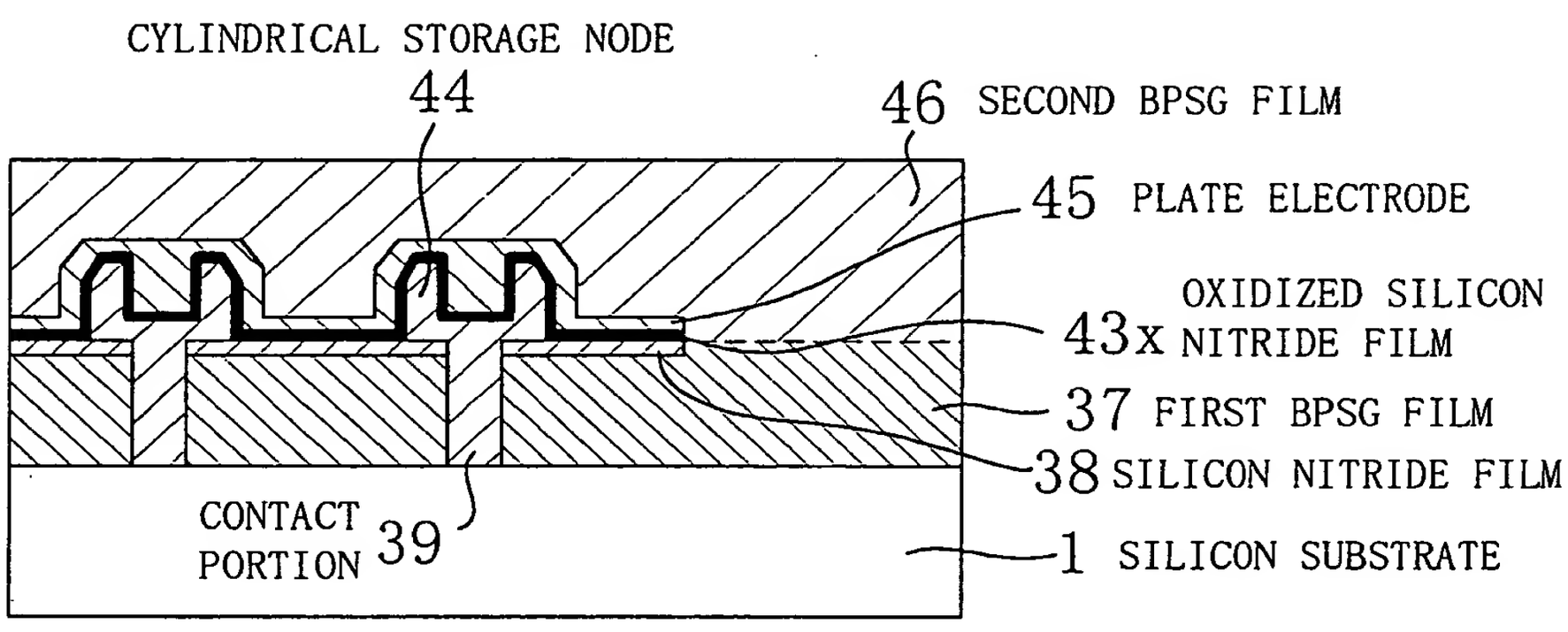
CYLINDRICAL STORAGE NODE
44
46 SECOND BPSG FILM
45 PLATE ELECTRODE
OXIDIZED SILICON
43x NITRIDE FILM
37 FIRST BPSG FILM
38 SILICON NITRIDE FILM
CONTACT PORTION 39
1 SILICON SUBSTRATE

Fig. 13(A)

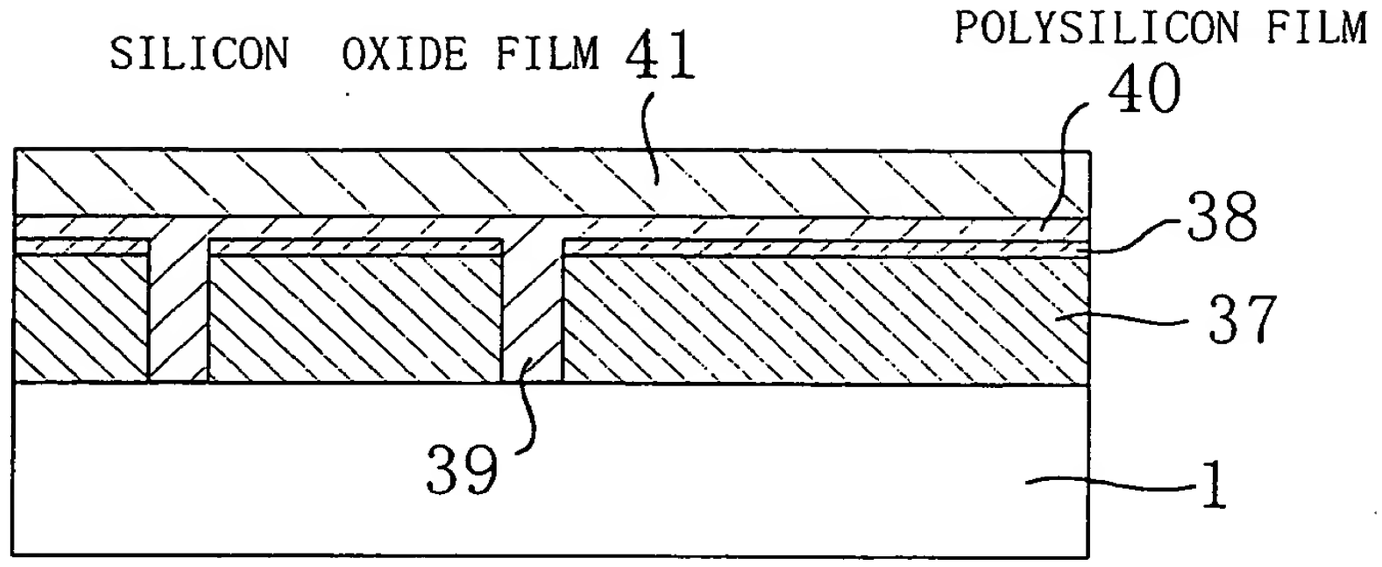

Fig. 13(B)

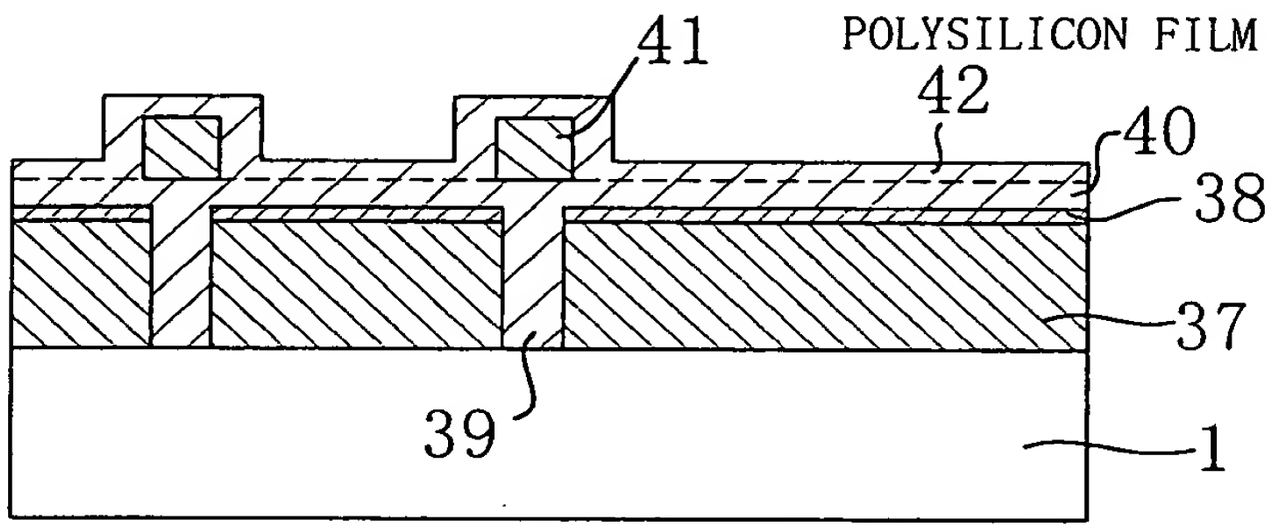

Fig. 13(C)

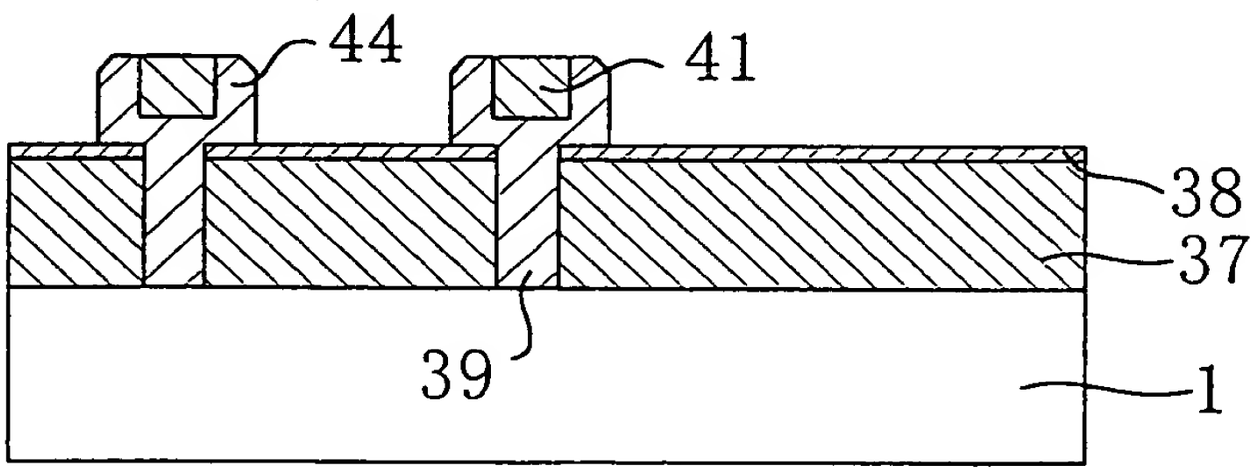

Fig. 13(D)

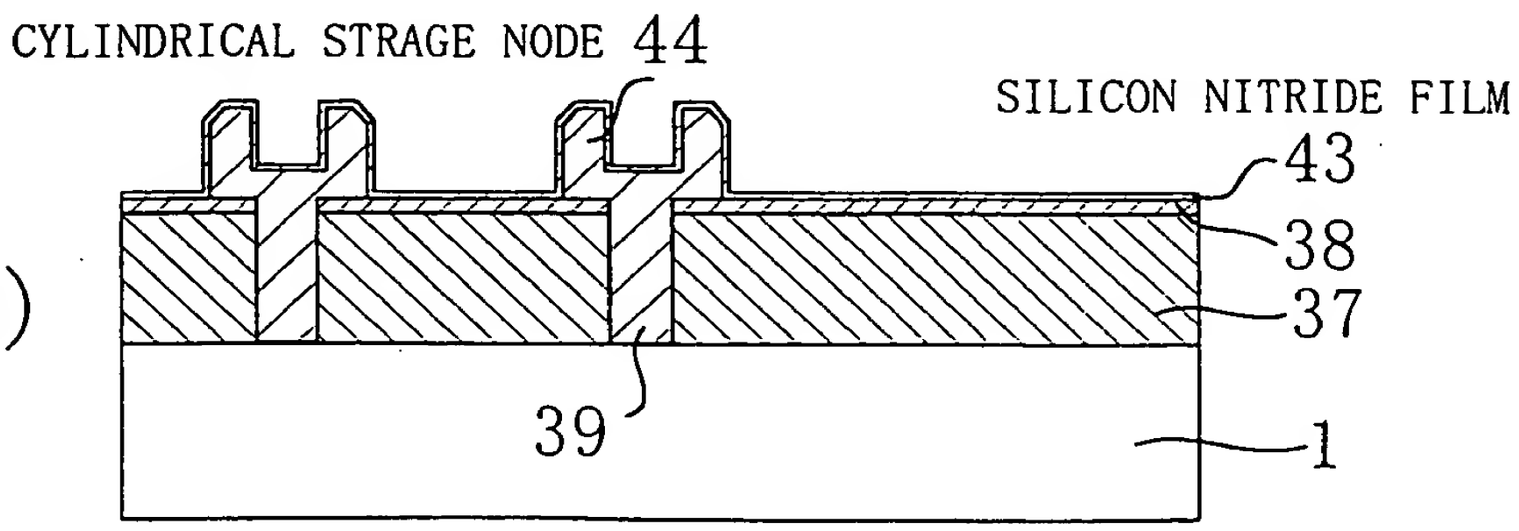

Fig. 14

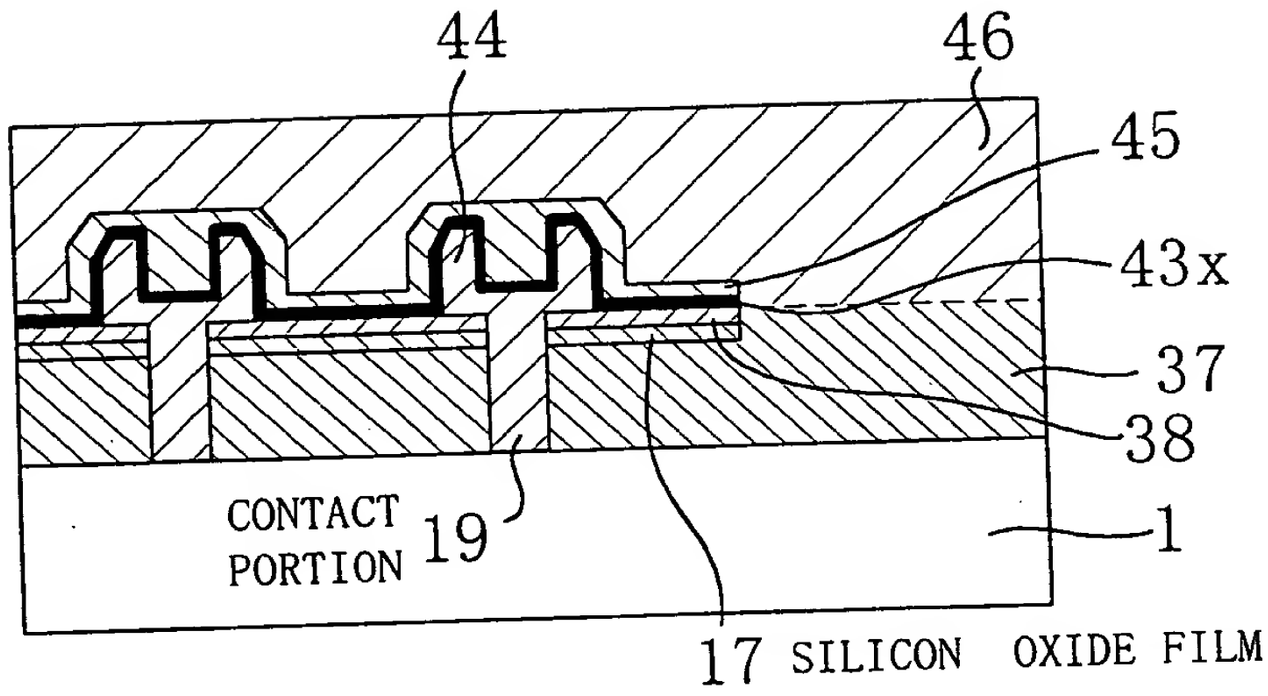

Fig. 15(A)

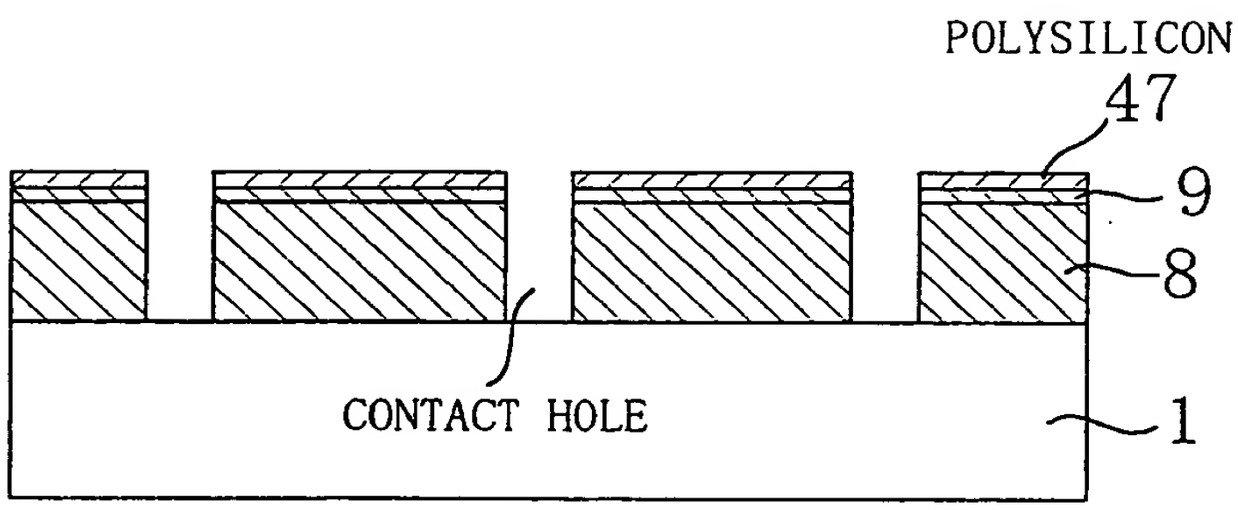

Fig. 15(B)

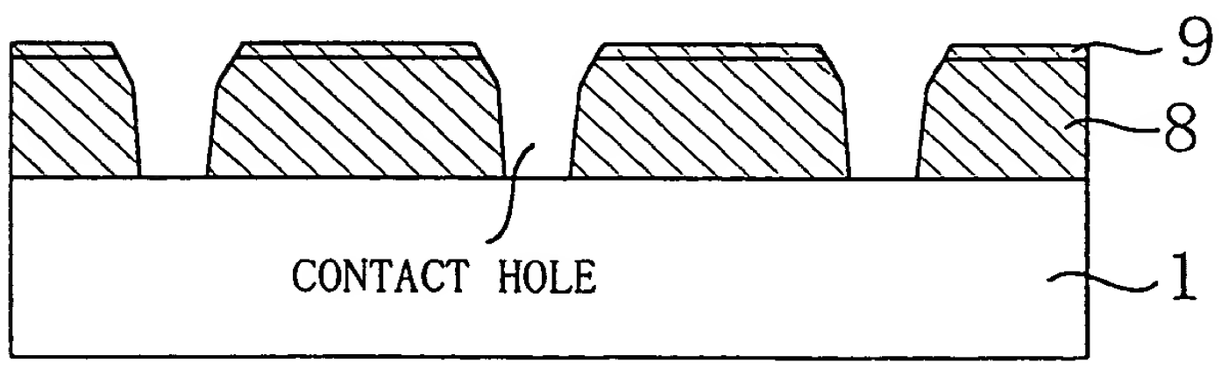

Fig. 16

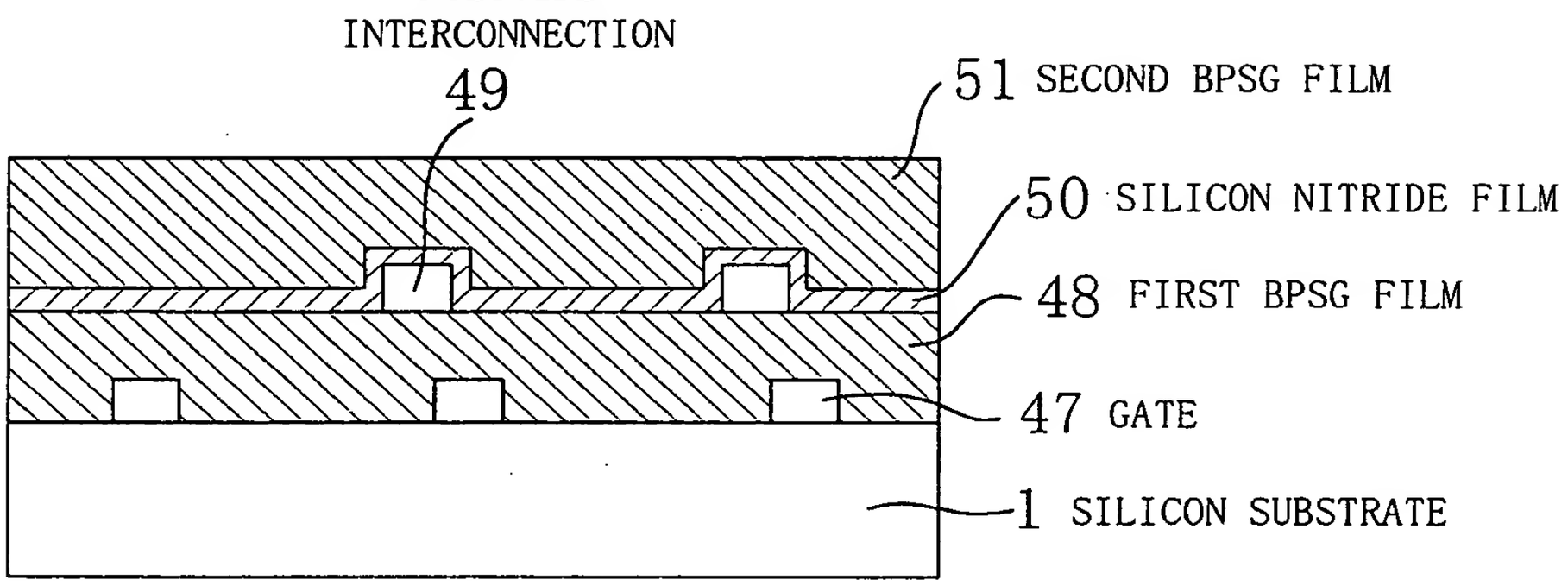
POLYCIDE
INTERCONNECTION
49
51 SECOND BPSG FILM
50 SILICON NITRIDE FILM
48 FIRST BPSG FILM
47 GATE
1 SILICON SUBSTRATE

Fig. 17

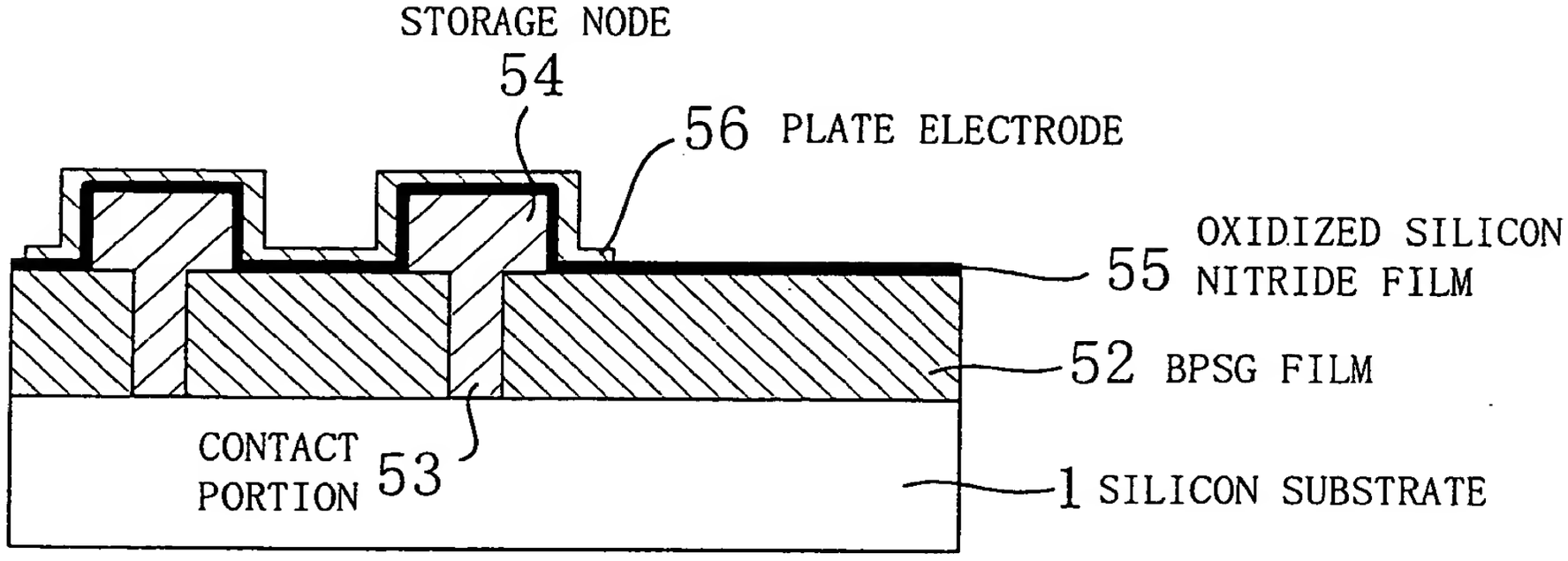
STORAGE NODE
54
56 PLATE ELECTRODE
OXIDIZED SILICON
55 NITRIDE FILM
52 BPSG FILM
CONTACT
PORTION 53
1 SILICON SUBSTRATE

Fig. 18

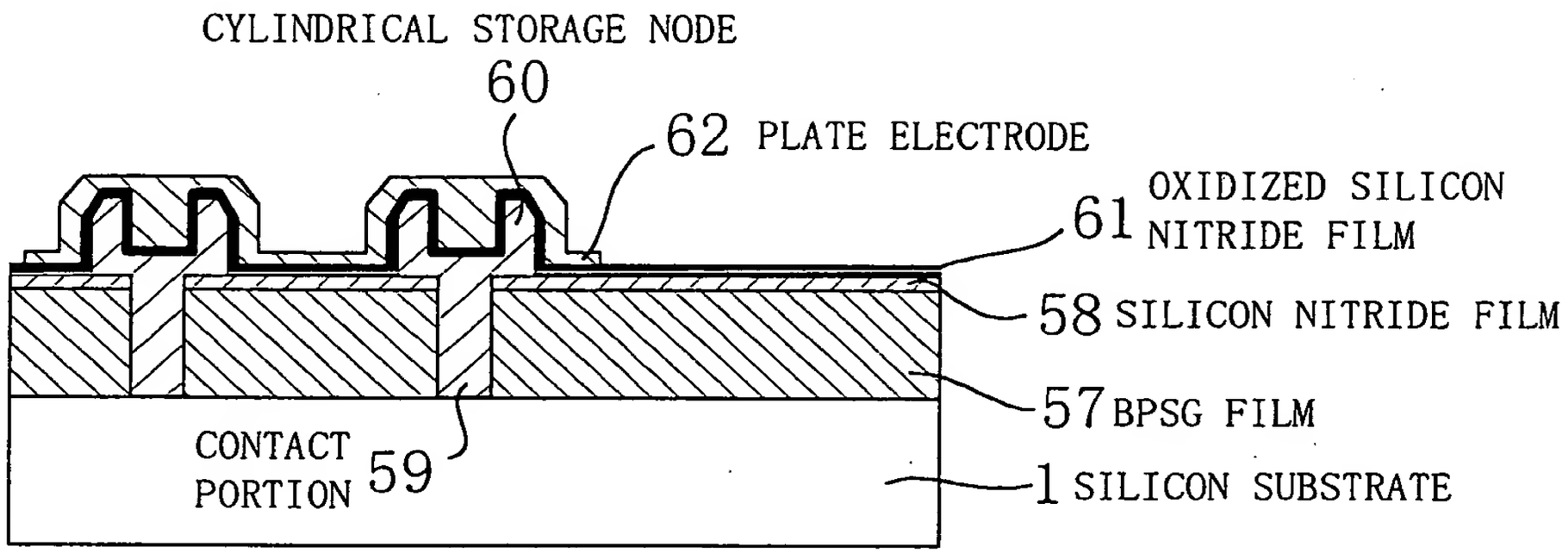
CYLINDRICAL STORAGE NODE
60
62 PLATE ELECTRODE
61 OXIDIZED SILICON NITRIDE FILM
58 SILICON NITRIDE FILM
57 BPSG FILM
1 SILICON SUBSTRATE
CONTACT PORTION 59

Fig. 19(A)

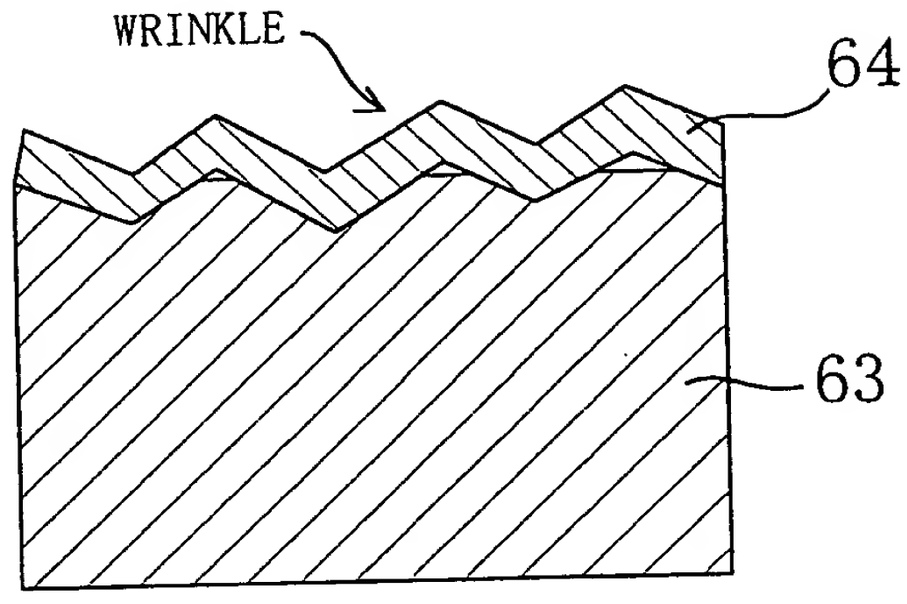

Fig. 19(B)